Flexible Readout and Integration Sensor (FRIS): New Class of Imaging Sensor Arrays Optimized for Air and Missile Defense

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Biological sensory organs operate at performance levels set by fundamental physical limits, under severe constraints of size, weight, and energy resources—the same constraints that many sensor devices have to meet.

Eyes are specialized sensory structures that extract information from the intensity, polarization, and spectral content of the light. Reliable and timely answers to the questions *Is there anything out there?*, *Where is it?*, and eventually, *What is it?* are the goals of all processing that follows the photoreceptor mosaics. This is in contrast to charge-coupled device (CCD) or complementary metal-oxide semiconductor (CMOS) video and still cameras that have been developed for the precise measurement of the spatial–temporal light intensity and color distribution, often within a fixed time interval, for accurate communication and reproduction in electronic or printed media. In this article, we present a bio-driven image sensor architecture that employs basic local processing for data reduction and information extraction (Fig. 1). It is presented here as an alternative approach to traditional analog readout integrated circuits (ROICs) with a special focus on infrared sensor arrays. Nonetheless, it is applicable to other wavebands as well.

One such application involves overhead and interceptor-based infrared focal plane arrays (FPAs), which are critical components of air and missile defense systems as well as for intelligence, surveillance, and reconnaissance applications. From a systems engineering perspective, optimizing these sensors is well justified. Nevertheless, current designs are limited by older analog and CCD technologies and have not gained much benefit from advances in digital technologies and Moore's Law. All the pixels are processed at all times, resulting in a significant computational load. The readout is slow and inflexible by current standards. The signal is restricted, leading to significant loss in temporal and dynamic range.

These sensors remain suboptimal despite the distinctive environment for these cases where all information of interest is embedded in only a few pixels (Fig. 2). The problem is more severe with large-megapixel, multispectral arrays.

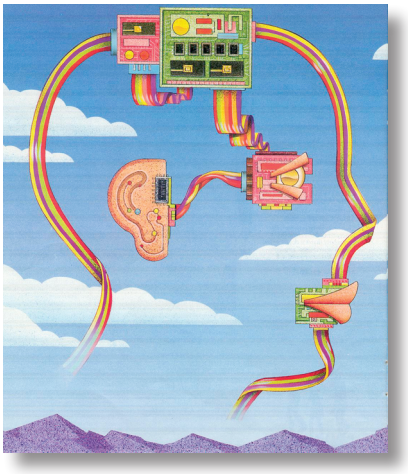

Figure 1. Pictorial of bio-inspired sensors.

The advances of CMOS technologies and, especially, the prospects of an on-chip hybrid analog-to-digital (A/D) system enable an alternative view and solution to sensor arrays for air and missile defense.

To address the uniqueness of this application, we outline a proposed solution that combines the initial steps (signal collection, digitization,

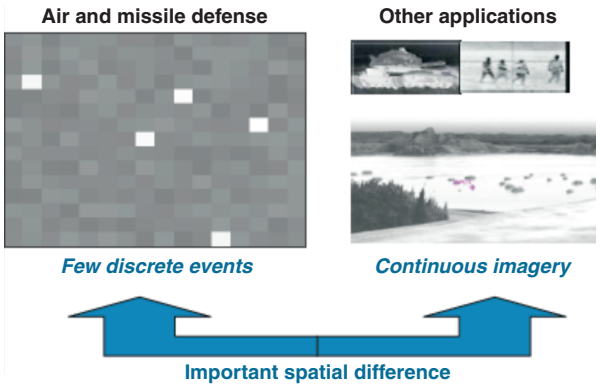

Figure 2. Typical infrared sceneries.

nonuniformity correction, and preliminary processing) of the signal processing chain onto the ROIC of the FPA (Fig. 3). As a result, only pixels of value (i.e., potential targets or new information) will be read off for further processing (discrimination and tracking). The new approach is more efficient because multiple functions are simultaneously implemented. Bottlenecks also are eliminated with greater functionality at the pixel level. In principle, the signals can be continuously accumulated, nonuniformity correction can be applied, image statistics can be calculated, and preliminary detections can be identified on the chip. In addition, the overall system's computational capability is increased and/or power requirements are reduced.

The all-digital event-based readout achieves ultimate flexibility in windowing or arbitrary pixel access at very high rates. It also eliminates the traditional analog shift register and Nyquist rate A/D converter. Therefore, it removes the upper limit on the frame rate as well as the conventional limits of electron well capacitance. Instead, the upper limit, and hence detection range, will depend on the environment radiance and the scene dynamics. For certain applications (sensor and environment), the proposed design will allow a significant increase in integration time while simultaneously reducing the processing and bandwidth requirements by orders of magnitude. Note that the input to the rest of the system can remain unchanged, and therefore the upgrade would be transparent (plug and play). This is a key feature to minimizing further development and integration costs.

Preliminary performance analysis of the concept on an element of the Ballistic Missile Defense System shows encouraging results. In addition, a proof of concept successfully demonstrated the near-term viability. The project lasted more than 3 years (2005–2007), and the results give further confidence. Three main objectives were achieved: on-chip programmable nonuniformity compensation, 26-bit dynamic range, and cryogenic operation. In addition, the following on-chip functionalities were proven: A/D at the pixel level, mean background level computation, programmable global reset, arbitrary readout (regions and/or pixels of interest) disabling dead pixels, and per-pixel threshold (Fig. 4).

With current and near-term CMOS technology, this approach potentially can result in a sensor array with up to 26-bit dynamic range, 10-kHz frame rate, and arbitrary windowing/readout capability. Such a sensor would be a modest technology leap but a potential game changer for system performance.

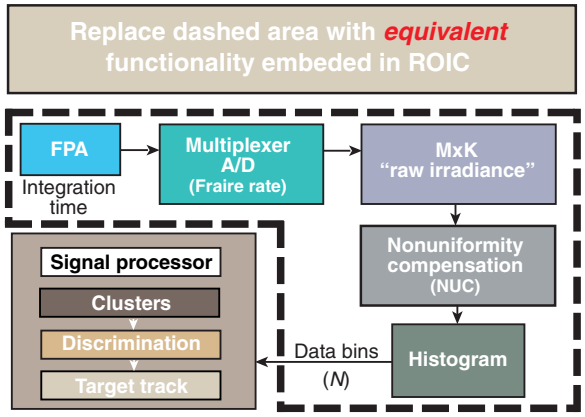

Figure 3. Block diagram for the video processing chain.

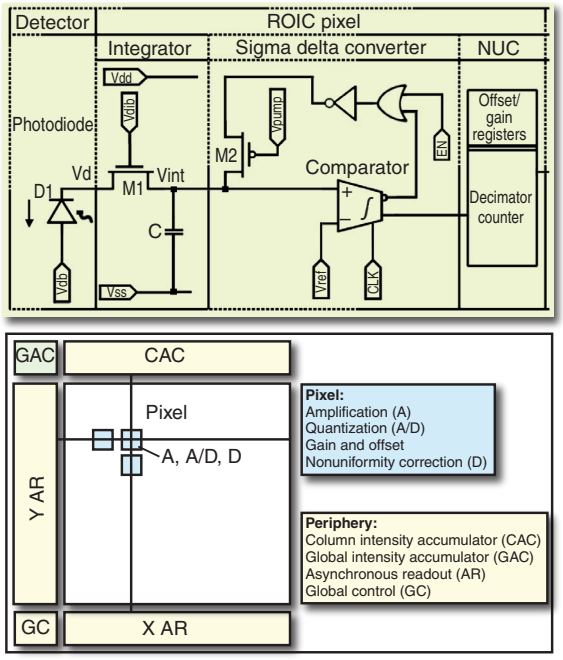

Figure 4. Pixel and chip architectures.

For further information on the work reported here, see the reference below or contact charbel.rizk@jhuapl.edu.

[1]Andreou, A. G., Pouliquen, P. O., and Rizk, C. G., "Noise Analysis and Comparison of Analog and Digital Readout Integrated Circuits for Infrared Focal Plane Arrays," in *Proc. of the 43rd Annu. Conf. on Information Sciences and Systems* (CISS09), Baltimore, MD, pp. 695–699 (18–20 Mar 2009).