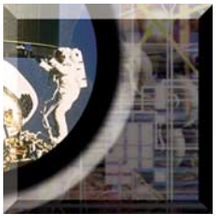

Evaluating and Implementing Commercial Processes for Producing Reliable, Cost-Effective Miniaturized Space Electronics

Sharon X. Ling, Binh Q. Le, and Ark L. Lew

Implementing commercial processes into the design of space electronics is a desirable, cost-effective way to leverage existing advanced packaging technologies derived from consumer electronics products. Demands for faster, better, lighter, and cheaper products have led to many innovative designs in commercial electronics, most noticeably in the telecommunications sector. But directly employing commercial processes in space applications, although cost-effective, is extremely risky. Therefore, careful studies and planning are critical to ensure the survivability of commercial processes throughout the space mission and full functionality under severe space environments. With many years of experience in developing high-reliability electronics, the APL Space Department began evaluating, qualifying, and developing commercial processes for space applications with chip-on-board (COB) technology. We have successfully demonstrated that our in-house fabrication and coating process can improve existing commercial COB technology to meet the stringent qualifications for space environments. Recently, we have focused on advanced interconnect methods such as flip chip technology and high-density printed wiring board development with blind and buried micro vias. These ongoing studies have demonstrated great potential for future space applications for both one-of-a-kind and build-to-print production runs.

INTRODUCTION

Satellite miniaturization not only makes space exploration more affordable, but also enables more global commercial space uses (e.g., telecommunications) and more advanced space explorations. The drive for smaller, lighter spacecraft has resulted in the need for the miniaturization of space electronics in terms of both size and weight without compromising the required reliability and functionality. On the other hand, commercial electronics products have pushed the electronic packaging market rapidly toward the almost exclusive use of advanced packaging schemes, e.g., micro ball grid array (μBGA), chip scale packaging, chip-on-board (COB), and flip chip (FC) technologies, in order to minimize size, weight, and cost (Fig. 1). In addition, the competitive and profitable consumer electronics market has made the use of the advanced packaging technologies very

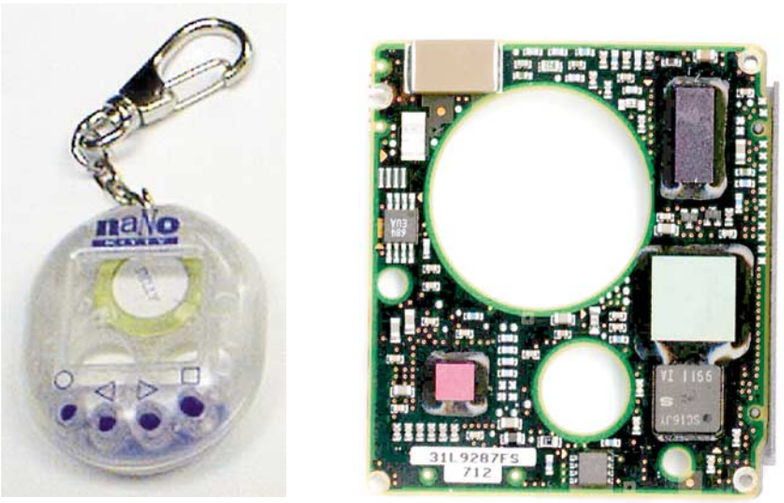

Figure 1. Commercial products implemented with COB and FC technologies: a popular toy (left) and a mini hard disk drive for a digital camera (right).

cost-effective. Therefore, it seems intrinsically necessary and beneficial to leverage commercial electronic packaging practices for space applications.

Nevertheless, well-developed and adequately supported commercial packaging schemes and processes cannot be applied directly to space electronics without comprehensive reliability studies. These studies are needed to ensure the functionality and integrity of electronics for space environments, which are often characterized by severe vibration during launch, substantial temperature fluctuation, and radiation degradation in orbit.

This article summarizes studies conducted at APL to leverage commercial electronic packaging and interconnect processes for potential space applications. Three advanced electronic packaging technologies are discussed: (1) COB, (2) FC, and (3) high-density interconnect with micro via printed wiring board (PWB). During the COB technology study (supported by APL IR&D funds), a unique coating process was developed and fully tested to support space applications. This process allows the rework of the miniaturized electronics, so necessary for one-of-a-kind and mass production. Studies of FC interconnect technologies and high-density PWB design with blind and buried microvias are also being conducted by APL to further improve commercial processes for high-reliability electronics. Although the latter studies are still in progress, test results are promising and have indicated great potential for space applications.

MINIATURIZATION TECHNOLOGIES

Chip-on-Board

COB technology involves mounting bare dies directly on a substrate—without an intervening package—to reduce the required substrate area and system weight. Using a conventional PWB as the substrate and wire bonding for interconnect, COB technology can yield a reduction factor of at least 10 in weight and volume.[1] It also reduces both the thermal and electrical resistances between the active die and the substrate, thus increasing circuit speed and improving assembly reliability.

COB technology, although used extensively in commercial products, has been considered only recently for space applications.[2] APL's COB technology development program, leveraged from both our high-reliability microelectronics and commercial processes, has emphasized cost, reliability, and suitability for such applications. Developing a COB process that can protect bare dies—from initial assembly to launch—and ensuring long-term survival in orbit are not simple tasks, especially when cost is a driving factor and the production volume is small. Our goal is to develop a reliable and repeatable process that can be reworked to minimize cost in low-volume applications as well as high-volume runs.

This multi-year research endeavor has been highlighted by several significant developments such as a die coating process, a unique COB wire bonding process on laminate substrates, and a unique process for individual die testing. We have successfully verified our die coating and wire bonding processes through extensive environmental tests and reliability assessments.[3] The implementation of COB technology, combined with custom, low-power, application-specific integrated circuit (IC) devices, has led to the development of a lightweight, low-power, low-cost multipurpose scientific imager (MSI)[4] and a modular, expandable command and data handling in your palm (C&DHIYP) device[5] in support of microsatellite development efforts. Our work has shown that APL's COB packaging technology can support a 10-fold reduction in size and weight as compared to more conventional techniques, and that the processes are reliable and repeatable for the construction of spaceflight electronics, in both large and small quantities. We believe that our COB technology is a potential candidate for technology transfer and will provide the credibility for APL to effectively interact in the commercial space electronics market.

Flip Chip

FC technology was invented in the 1960s at IBM with the introduction of the C4 (controlled collapse chip connector) process.[6] In FC assembly, the bumps

(solder, gold, etc.) are placed on the chip bonding pads (I/O), and the bare die is then turned upside down to form an interconnection between the die and the substrate through various reflow and bonding techniques. FC technology supports high-density interconnection without compromising component size or weight since it uses the entire area underneath the die rather than just its periphery for interconnection. It can also achieve better performance, higher reliability, and, with the development of new materials and processes, lower cost.

The Space Department, funded by the NASA Advanced Technology Development (ATD) Program, initiated studies in 1999 and 2000 to assess the appropriateness and reliability of three types of emerging FC interconnect technologies for space applications: (1) anisotropic conductive adhesive (ACA) with gold/nickel (Au/Ni) bumped dies,[7] (2) nonconductive paste (NCP) with Au stud bumped dies,[8] and (3) isotropic conductive paste (ICP) with Au stud bumped dies.[9] (Conventional solder processes were used as controls.) These studies focused on the reliability of the interconnections between ICs and the substrate because they appear to be the potential weak links for long-term reliability.[10]

These alternative interconnect techniques were selected for several reasons.

- Potential for smaller, thinner, and lighter products. Solder bridging and brittle intermetallic formation can be avoided to permit higher I/O density.
- Applicable for flexible substrate and temperature-sensitive components. Some of the interconnect materials can be cured at lower temperatures than solder, or even with ultraviolet light.
- Similar to conventional solder interconnects in process procedures. Some combinations of the die bump metallurgy and interconnect materials can achieve both electrical interconnection and mechanical strain relief in a single process. This eliminates the entire step of underfilling (injecting underfill material between the component and the substrate after formation of the interconnections), a process widely used in surface-mount technology to increase the assembly's fatigue life. The simplified process can result in shorter assembly time and therefore cost savings.
- Feasible for large- and small-quantity spacecraft electronics products. Unlike the conventional solder bumping process that requires the entire wafer, Au stud bumps can be performed on individual dies. This advance could result in significant cost savings, especially when only small quantities are needed.
- Potential for better performance in terms of electrical, structural, and thermal behavior.
- Environmentally benign since lead contamination from the traditional Sn/Pb solder materials is avoided.

Assembly Techniques

ACA is an interconnect material in which fine conductive particles are suspended throughout the nonconductive epoxy matrix. It is an electrical isolator at room temperature. During assembly, conductive particles are trapped between the Au/Ni-plated bond pads on the die and the traces on the PWB (Fig. 2a). With applied pressure and elevated temperature, an electrically conductive path is formed between the bump and the pad by the physical contact of conductive particles and through tunneling effects; electrical isolation is maintained in the in-plane direction. The remaining ACA material underneath the die serves as underfill for mechanical strain relief.

Using Au stud bumped dies with NCPs is another simple, cost-effective method to interconnect FC dies to the substrate. This process employs standard wire bonding equipment to provide ball bonds on the bare die bond pads. The tails of the wires are then cut off by the bonding machine, leaving the Au studs on the die surface ready for the next assembly (Fig. 2b). During assembly, under pressure and heat, the Au stud bumps penetrate the NCP material and form electrical connectivity through metal-to-metal contact; meanwhile, the cured NCP provides mechanical bonding and strain relief, eliminating the need for an additional underfill process. Perhaps the most intriguing characteristic of this technology for space applications is that the preparation of bond pad metallurgy can be performed on individual dies instead of the entire wafer. This could result in a significant cost saving when only a small quantity of dies is needed, a typical scenario for space electronics, and even greater savings for mass production runs (e.g., communications satellites).

The FC assembly procedures with ACA and NCP are similar. Interconnect material in paste form is first dispensed on the PWB using a syringe or a stencil. For smaller dies, syringe dispensing in cross or dot patterns is sufficient to allow complete flow of the material to the corner of the die during adhesive curing and to form a well-shaped fillet around the die. For larger dies, however, the shape of the paste dispensed from the syringe becomes critical. In that case, a stencil might be necessary for dispensing the paste material to induce even flow during assembly. The FC dies are then aligned with the conductors on the board through a split-mirror visual system or some other technique on the die bonder. Pressure is applied and maintained while the temperature of both the lower and upper chucks of the bonder rises to allow the interconnect material to reach its curing temperature. However, the applied pressure must be high enough to induce plastic deformation of the conductive particles to form reliable interconnection,[7] without causing damage to the bumps.

Conversely, ICP material is electrically conductive. The Au stud bumps, prepared similarly using a wire

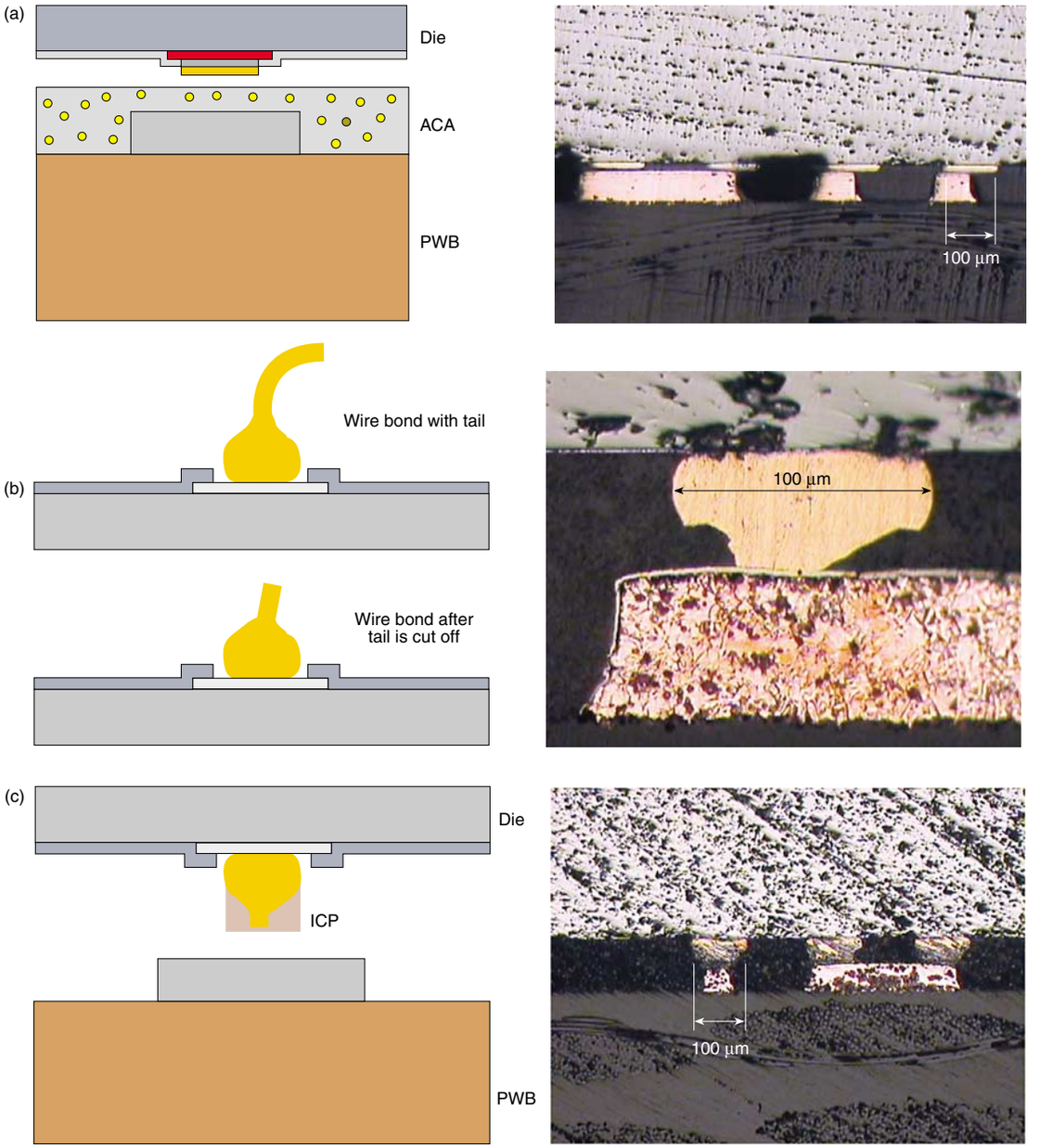

Figure 2. Alternative FC interconnect technologies: (a) Au/Ni-plated FC die using ACA and underfill, (b) Au stud bumped FC die (without coining) using NCP, and (c) Au stud bumped FC die (with coining) using ICP and underfill.

bonding machine, must be coined for ICP interconnections in order to leave flat surfaces where the ICP material is coated before assembly (Fig. 2c). Because the height of the Au stud bump after coining is around 70 μm, the thickness of the ICP coating is chosen to be 35 μm. The paste is screened on a flat surface with the desired height. The Au stud bumped dies are dipped in the paste to coat the ICP material. All of the dies are placed on the PWB using a pick-and-place machine, and the assembly is then cured in an oven according to the material specification. The electrical interconnection is established through the ICP material, which, at the same time, also provides the thermal path. The underfilling process is necessary in this interconnecting technique to accommodate the coefficient of thermal expansion (CTE) mismatch between the silicon die and the PWB.

A study of the various FC technologies on rigid polyimide PWB was jointly conducted with an APL subcontractor, Fraunhofer Institute of Reliability and Microintegration (IZM), Berlin, Germany. Manufacturing cycle times and costs per 5 × 5 mm dies for FC interconnect technologies using ACA, NCP, and ICP were estimated

and compared. It can be concluded that, while the unit cost is comparable for all three technologies, savings in assembly cycle time using ACA and NCP have proven to be significant, especially in mass production. (Interested readers should see Ref. 11 for details.)

Conductive adhesive joining technology has been used for many years in chip-on-glass application for LCD displays because the LCD material cannot withstand solder reflow temperature, and the indium tin oxide metallization of the LCD display is not compatible with the solder.[12] Only recently have efforts been made to implement adhesive joining technology in low-cost FC bonding. The advantages of adhesive FC interconnect technologies are so appealing that industries have been rapidly incorporating them into their commercial products. ACAs are used for FC assembly with pitch as small as 70 μm.[13] The Casio MR-80 radio is claimed to be the first to use ACA FC interconnection in a credit card–sized AM/FM package (Fig. 3). Conductive adhesive is used for FC assembly by Matsushita Electric Industrial, Fujitsu, and Hitachi; anisotropic conductive films are used in Casio computers.

Reliability Assessment

Unlike solder interconnect, whose physical, mechanical, electrical, and thermal behaviors have been thoroughly studied, long-term reliability carefully examined, and failure mechanisms sufficiently understood,[14,15] the long-term reliability of the adhesive FC interconnection technology, especially in severe space environments, has not been thoroughly investigated. Moreover, new interconnect materials with better properties and improved performances[16,17] make the process of reliability evaluation and qualification a continuous pursuit. In order to evaluate the state-of-the-art advanced FC interconnect technologies for possible insertion in space applications, APL has established a comprehensive test plan to assess long-term reliability using a suite of reliability tests and analyses.

To support reliability analyses, we developed test board assemblies using two sizes of bare dies: a 5 × 5 mm die with a peripheral I/O count of 84 and a 10 × 10 mm die with a peripheral I/O count of 184. The pitch of the die is 200 μm (100-μm line/100-μm spacing), the bond pad size is 100 μm, and the passivation openings are 80 μm. Both types of dies have built-in 4-point and daisy-chained 2-point resistivity measurement structures. The former allows accurate resistivity measurement of a single joint, while the latter is used to check electrical connectivity throughout the die.

The glass-reinforced polyimide test boards are 89 × 89 mm in size and 1.57 mm in thickness. Each board accommodates four 5 × 5 mm dies and two 10 × 10 mm dies. Figure 4 shows an FC assembly test board. Signals are routed through three 50-pin edge connectors that enable *in situ* resistance measurements.

Many factors can affect the feasibility and quality of adhesive FC bonding. In addition to the various types of bump metallurgy, the selection of interconnect material is also crucial. Material properties (e.g., CTE, mechanical strength, viscosity, electrical conductivity, insulation resistivity, glass transition temperature, pot life) can all

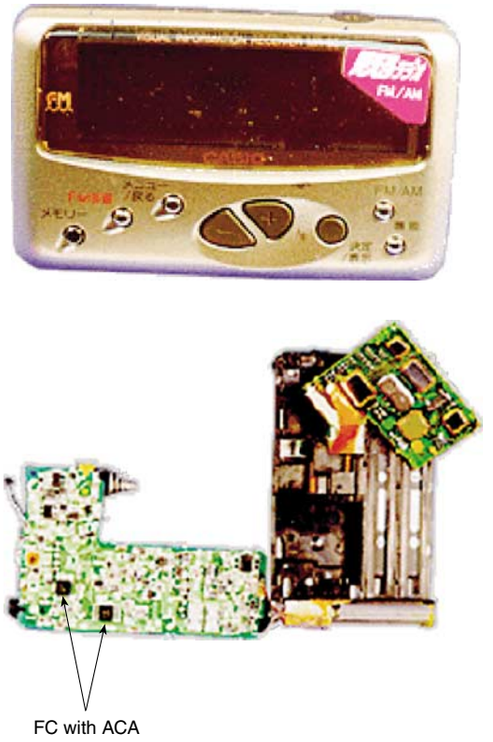

Figure 3. Casio MR-80 radio with ACA assembly (source: Prismark/IEEC, 1997).

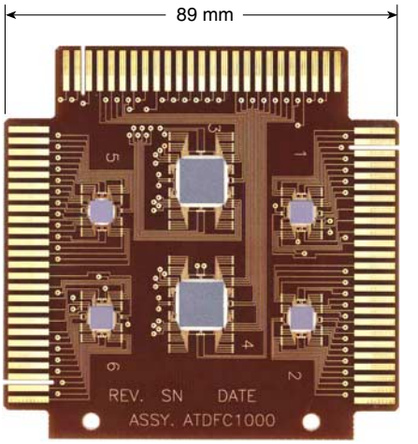

Figure 4. FC test board used for *in situ* resistance measurements.

impact successful and reliable FC bonding. Assembly parameters (e.g., curing temperature, time, and pressure) are also critical. The FC test coupon assembly matrix for this study is summarized in Table 1. The adhesive materials were selected based on a search of the literature, a material properties survey, and our past experiences. Different curing schedules were also chosen to quantify the impact of assembly parameters on the quality of interconnects.

The PWB has been designed to accommodate three edge connectors to facilitate *in situ* resistance measurements during reliability tests. A schematic of the test setup is shown in Fig. 5. One pair of relays in each of the multiplexer modules is switched simultaneously to

Table 1. Assembly matrix of the FC interconnect technologies.

Material	Conductive agent	Curing schedule	Die metallurgy
ACA #1	3-μm Au-coated polymer	10 s @ 250°C 15 s @ 220°C	Ni/Au plated
ACA #2	6-μm Ni sphere	30 s @ 200°C 60 s @ 180°C	Ni/Au plated
NCP #1	None	10 s @ 200°C 15 s @ 180°C	Au stud bumped, without coining
ICP #1	Ag	30 min @ 150°C	Au stud bumped, with coining
ICP #2	Conductive polymer	15 min @ 130°C	Au stud bumped, with coining
Solder	Sn/Pb	Reflow: 30 s @ 240°C	Solder bumped

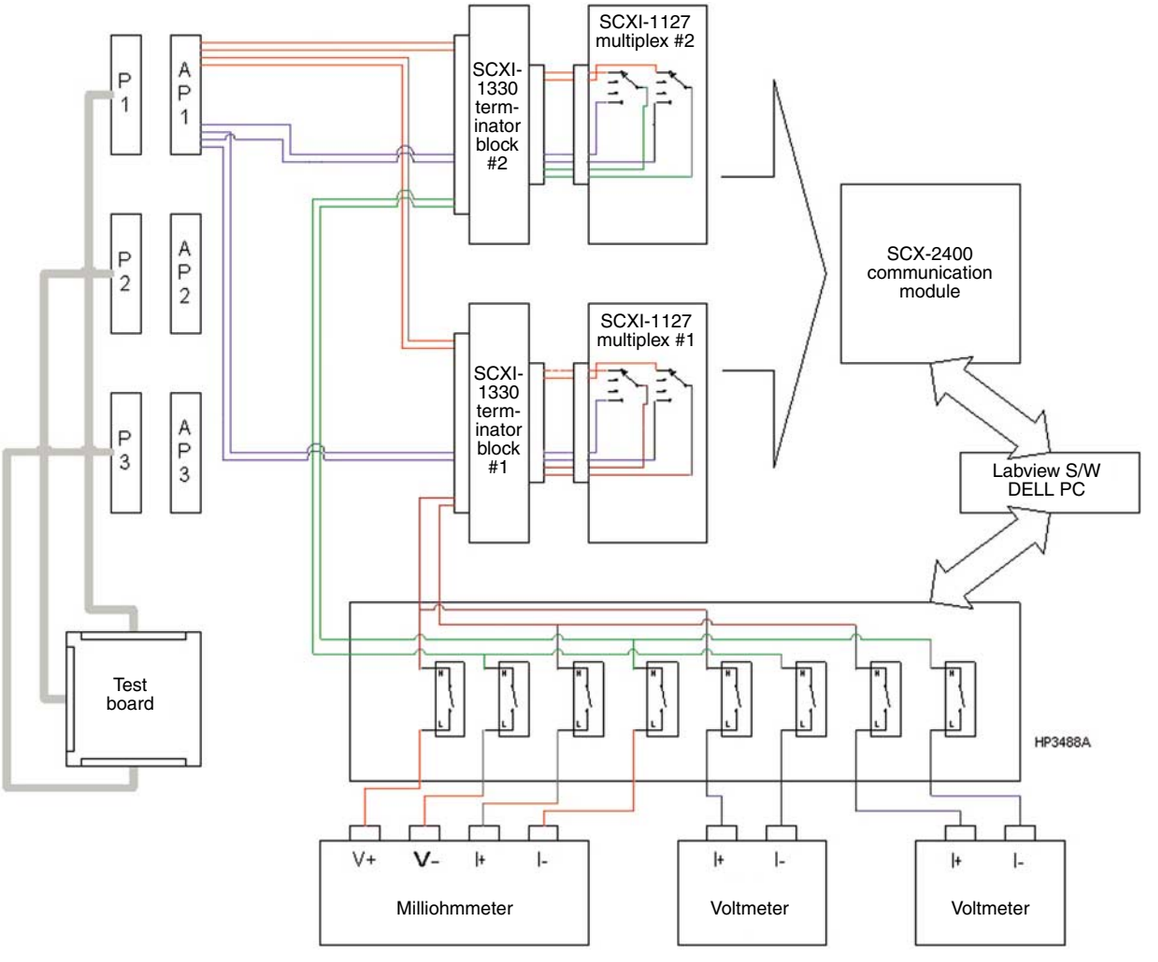

Figure 5. Schematic of the test setup for *in situ* resistance measurements (P = mass terminator connectors from edge connectors, A = mass terminator connectors).

enable one 4-point resistance measurement using a milliohmmeter. The switching sequence continues until all the 4-point measurements are taken from six dies on the board. Voltmeters are then triggered for 2-point resistance measurement. Owing to the two-wire mode setting of the multiplexer, two digital voltmeters are needed in this test setup, and two electrical continuity measurements are taken at a time. A joint is considered to fail when its resistance value increases 10 times. All measured resistance data are stored in the computer for postprocessing.

Anomalies were observed during the assembly using ICP and underfill. With ICP #1, none of the 10 × 10 mm dies adhered to the board. The smaller dies remained on the board but showed poor adhesion when underfill was applied. Inspection of the interconnection area showed a cohesive failure for this ICP (Fig. 6). The Au stud bumped die assembly with ICP #2 revealed similar results. In general, dies appeared to have poor adhesion to the conductor on the PWB. A photograph of a micro section of a failed assembly (Fig. 7) shows an interface crack between the die and the conductor. The standard stud bump bonding process of Matsushita, which is similar to the Au stud bumped die with ICP FC interconnect technology investigated in this study, was successful on both ceramic and organic substrates.[8] It was suspected that PWB local warpage could have caused the assembly failure. The thin ICP coating layer on top of the Au stud bumps worsens the situation by providing insufficient peeling resistance while the board deforms during adhesive curing. An alternative ICP material with a lower curing temperature and shorter curing time may solve the assembly difficulties.

A 1000-thermal-cycle test has been conducted on the test boards. A –55 to 125°C temperature range was selected with a 4°C/min ramping rate. The dwell time was 30 min at each temperature extreme. Although the operational temperature for typical space electronics is well maintained with far less excursions, the larger temperature range for the reliability test was selected to induce and accelerate failures in the FC interconnections. Based on test results, it can be concluded that appropriate interconnect material selection, FC die preparation, FC bonder capability and accuracy, and PWB quality are all major factors dictating the quality of FC joints. However, assembly parameters, process control, and human factors may have an even greater influence on joint quality.

Despite limited funding and experience in FC assembly, some of the FC test boards that we have successfully assembled have shown promising results. The daisy-chained resistance measurement for the Au stud bumped die FC assembly using NCP material, as well as for the Au/Ni-plated die FC assembly using ACA #1, remained stable after 1000 cycles. Single-joint resistance measured by the 4-point test structure remained steady in the microohm range.

Table 2 shows reliability test results in the form of numbers of interconnect failures as a function of temperature cycles for the various FC interconnection technologies. Three companies, along with APL, assembled the FC test boards with selective interconnection technologies using the same test dies, test boards, and interconnect materials. Again, a joint was considered to have failed when its resistance value increased 10 times. There were 30 data points for each test coupon. More detailed assessments, including micro sectioning, will be conducted to evaluate and confirm failure mechanisms.

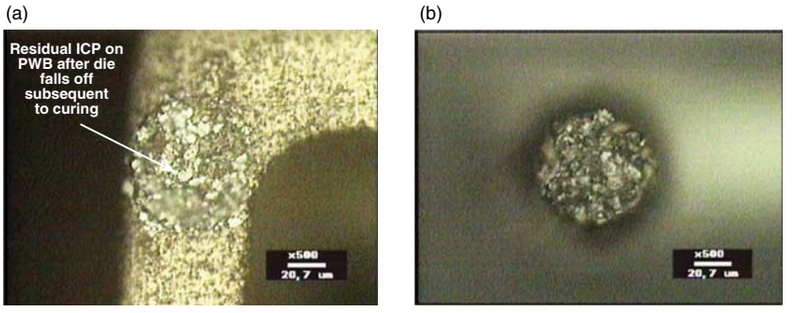

Figure 6. Magnifications showing (a) poor adhesion of Au stud bump to the conductor on the PWB and (b) Au stud bump coated with ICP #1 after separation.

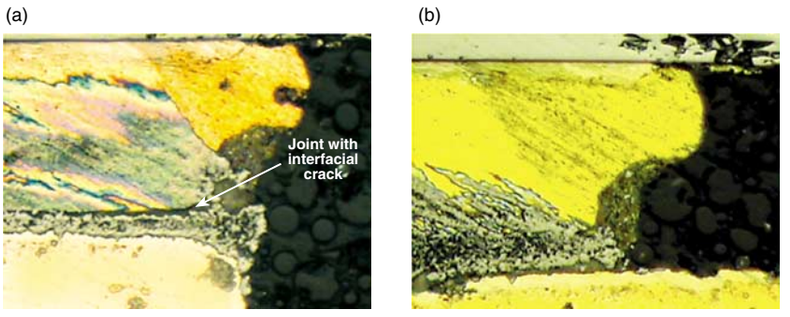

Figure 7. Comparison showing (a) an interface crack between the Au stud and the conductor on the PWB and (b) a good Au stud joint coated with ICP #2.

Microvias

The previous discussions on COB and FC addressed component miniaturization. The second area for miniaturization of electronics is in the development of substrates or PWBs.

Table 2. FC interconnect technology reliability test results (number of failures as a function of temperature cycle).

FC interconnect technology	Assembly performer	Temperature cycles 0	100	200	300	400	500	600	700	800	900	1000
Au stud bumped	APL	0	1	1	2	3	4	4	5	5	5	5
die (without	Company B	2	8	8	9	10	13	13	15	15	16	16
coining) with	Company C	9	9	9	9	10	11	11	11	11	11	11
NCP #1	Company D	0	2	2	2	2	3	3	3	3	3	3
Au/Ni bumped	APL	0	0	0	1	2	3	3	3	3	3	3
die with ACA #1	Company B	0	0	3	3	5	6	6	6	6	6	6
	Company C	15	15	16	16	17	18	18	18	18	18	18
	Company D	0	1	1	1	2	4	4	4	4	4	4
Au/Ni bumped	APL	6	23	26	28	29	29	29	29	29	29	29
die with ACA #2	Company B	2	16	16	18	18	19	20	20	20	20	20

Although not as "glamorous" as dealing with micrometer feature sizes, substrate design plays an important role in miniaturization. The rapid progress in ultra-high-density ICs and advanced interconnect schemes (e.g., COB and FC technologies) cannot be implemented without advances in compatible and reliable high-density PWB development. To support this project, the Space Department, in collaboration with the APL Technical Services Department, has been conducting a multi-year study to investigate the methodologies and assess the reliability of micro vias in low-cost, high-density PWB design. This effort takes advantage of our in-house MIL-qualified PWB fabrication facilities.[18] Our goal is to qualify and implement the high-density interconnect techniques with micro vias in PWB design to reduce space electronic system weight and volume.

In multilayer PWB design, plated through holes (PTHs), with a typical size of 0.4 mm, interconnect signals from one layer to another. The integrity of the PTHs is the most important aspect in high-reliability PWB design. Reliable PHT development requires proper process control to maintain the consistent plating thickness of the copper wall and the strength of the interface between the internal traces and the PTHs. As the number of PTHs increases with respect to the complexity in PWB design, areas available for mounting active components are minimized. To support high-density electronics, advanced PWB design with blind and buried vias is used in addition to PTHs. Blind vias provide interconnections from the external signal layer to an internal one; buried vias interconnect only internal signal layers.

Figure 8 shows a cross section of a PWB with blind and through-hole vias. Both blind and buried vias can effectively divert signals from high-I/O-density ICs for routing without compromising significant board surface area, especially when implemented with area array ICs such as FC and μBGA. With reduced PTH size, blind and buried vias in PWB design are the most effective way to further increase available surface area for supporting electronic components, thus reducing the overall system weight. For typical micro vias, the hole sizes range from 0.05 to 0.25 mm. In conventional PWB fabrication, mechanical drilling is used with via sizes greater than 0.25 mm. For smaller holes, laser-drilling processes are required.

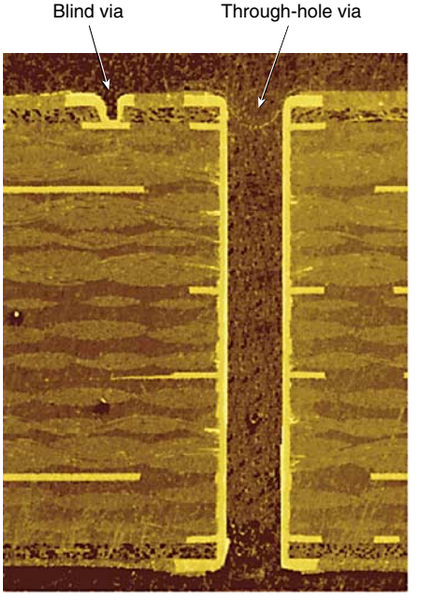

Figure 8. Cross section of a PWB with a 1.5-mm laser-drilled blind via and a 0.40-mm mechanically drilled through hole.

Forming Processes

Two laser drilling processes, conformal mask drilling and full via formation drilling, were evaluated. In the former, the external copper is chemically pre-etched using a photolithographic process to expose the dielectric layer. A CO_2 laser beam is then focused on the surface of the PWB to ablate the dielectric material and thus form the via hole. A postdrill cleaning with plasma etching prior to electroless copper plating is required for conformal-mask drilling to ensure a clean surface for subsequent plating steps. The full via formation drilling process uses dual laser sources, UV and CO_2. The UV source is used for ablating the copper layer, and the CO_2 laser is used subsequently to ablate the dielectric material to form the vias. A postdrill cleaning prior to electroless copper plating is also needed. The potential advantage of the full via formation drilling process is the elimination of the tedious inspection step required in the conformal mask drilling process to ensure proper removal of copper before laser drilling.

Electroless deposition of copper after the drilling and cleaning of via holes is a critical step in high-quality microvia fabrication. Two plating processes—conventional DC and pulse—are being evaluated in this study. In the pulse plating process, the supplied electrical input is turned on and off repetitively with adjustable duty cycle and frequency. The agitated/regulated current induces more even ion distribution, which leads to better copper ion deposition and plating quality for blind holes with high aspect ratio. In general, the aspect ratio is considered to be high when the ratio of the depth and diameter of a blind via exceeds 10.

Reliability Assessment

To support the study of micro via designs, test boards constructed from polyimide as well as epoxy glass materials with daisy-chained blind and buried vias (Fig. 9) have been fabricated to conduct a reliability assessment. Blind and buried vias with hole diameters varying from 0.08 to 0.30 mm (each diameter being associated with various annular ring sizes) are implemented in the test board design. Buried vias have both the filled and unfilled configurations. In the filled configuration, conductive epoxy is forced into the vias before the final lamination of all PWB layers. This process eliminates the potential reliability concern of void formation in the vias when the prepreg material is inadequate to fill the vias during lamination.

The test boards were subjected to a 1000-thermal-cyle test from –55 to 125°C. Microsection inspections of the test coupons and the as-built PWBs were performed. Figure 10a shows a failed microvia with a 0.08-mm diameter. The via was overetched during the postcleaning procedure after laser drilling, and the restricted opening area prevented uniform copper plating. Preliminary test results indicated that microvias larger than 0.15 mm are reliable (Fig. 10b) and are capable of supporting space missions. Figures 11 and 12 plot the resistance values versus numbers of cycles for blind and buried vias with polyimide and epoxy glass PWBs, respectively.

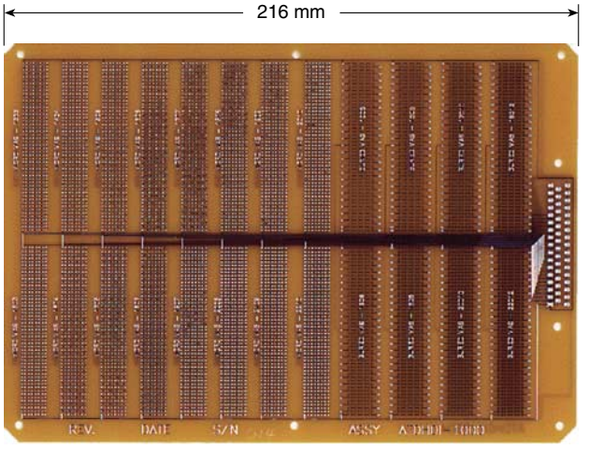

Figure 9. High-density interconnect test board with daisy-chained micro blind and buried vias.

CONCLUSION

The successful development of our in-house COB coating process led to the space qualification of a commercially available microelectronic packaging process and shifted the space electronics design and implementation at APL into a new paradigm. Leveraging commercial electronic packaging techniques and interconnection processes for potential space application was proven to be not only possible, but indeed favorable for the significant advantages of weight, size, and cost savings. In fact, it may prove to be the preferred path

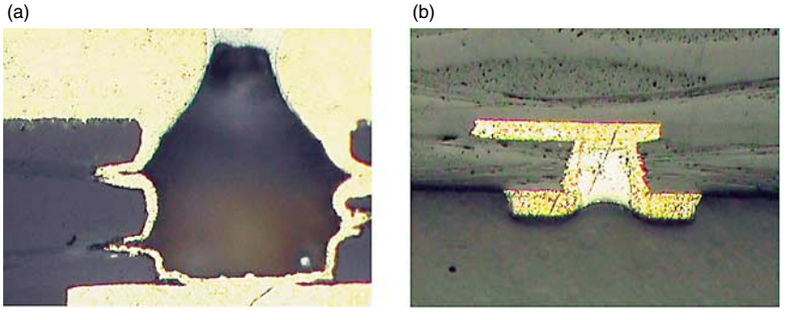

Figure 10. Comparison showing (a) a cross section of a failed 0.08-mm blind via and (b) a good 0.15-mm blind via.

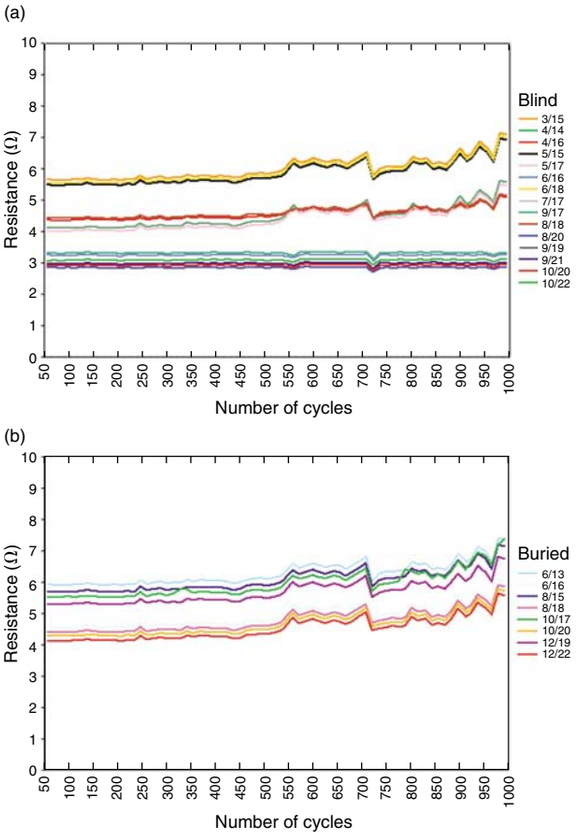

Figure 11. Reliability test results for (a) blind and (b) buried vias with polyimide PWB. (The first number in the legend denotes the diameter of the via and the second denotes the diameter of the annular ring, both in mils.)

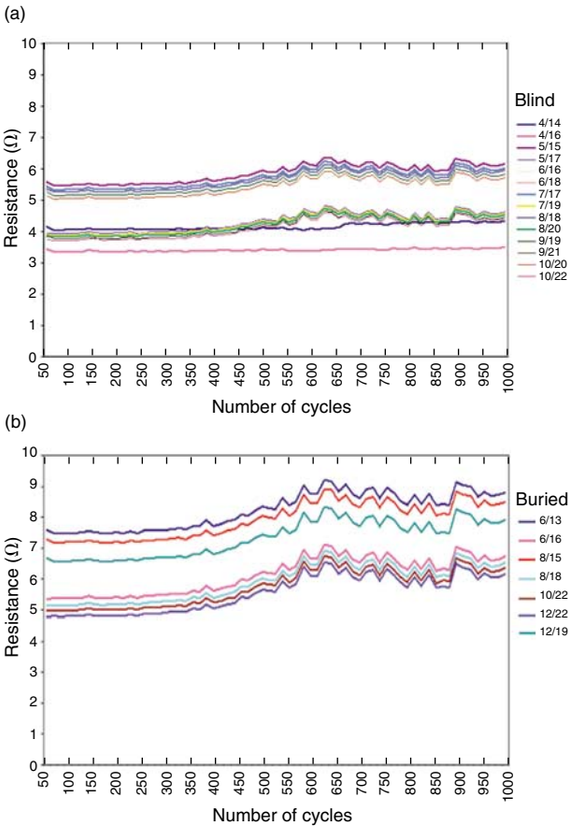

Figure 12. Reliability test results for (a) blind and (b) buried vias with epoxy glass PWB. (The first number in the legend denotes the diameter of the via and the second denotes the diameter of the annular ring, both in mils.)

for space electronics miniaturization and ultimately for spacecraft miniaturization. These technologies will also be attractive for both one-of-a-kind and production-run commercial space product suppliers and satellite providers. The FC interconnect technology evaluation and the PWB with micro vias study have followed the successful COB qualification and implementation efforts in the Space Department. Although the test results from these two studies are still being gathered and analyzed, already there have been strong indications that some of the technologies have the potential for implementation in space electronics design.

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ACKNOWLEDGMENT: The authors acknowledge the APL Technical Services Department, IZM, HyComp, and Toshiba Inc. for their support in the fabrication and assembly of test articles as well as NASA for providing funding for the studies.

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