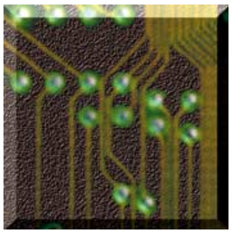

The Engineering, Design, and Fabrication Facility: A Unique APL Resource

Harry K. Charles, Jr., and Joel A. Weiner

The Engineering, Design, and Fabrication (EDF) Facility is a unique resource providing a wide range of development, engineering, design, fabrication, and testing services for APL and its external customers. The facility consists of modern laboratories and specialized equipment and processes. It is staffed by skilled engineers, scientists, technicians, and craftspeople, all dedicated to the production of high-quality electronic, electromechanical, and mechanical hardware. The EDF is a flexible, dynamic resource that responds rapidly to customer needs in both traditional and new business arenas. With its technology and personnel, the EDF is poised to deliver advanced services and hardware for many years to come. (Keywords: Electronic services, Engineering design, Fabrication, Hardware, Mechanical and material services, Prototyping.)

INTRODUCTION

The Engineering, Design, and Fabrication Facility (EDF) of the Technical Services Department (TSD) is an integrated Laboratory resource for the development, design, fabrication, testing, and qualification of prototype, one-of-a-kind, and limited-quantity advanced electronic, electromechanical, and mechanical hardware. The facility consists of extensive equipment and laboratory resources, coupled with the expertise of skilled scientists, engineers, technicians, and craftspeople. It also maintains almost 200 standard processes and procedures that capture detailed design and fabrication knowledge to facilitate project documentation and technology transfer. These resources reside primarily in TSD's Electronic Services Group (TSE) and Mechanical Services Group (TSM); additional support comes from the Department's computer and information systems services (especially computer-aided engineering) and fiscal administration. The groups are functionally aligned, with a minimum of overlap and service duplication. Figure 1 illustrates the major facility capabilities and service functions. Further details of EDF services can be found in articles by Hider et al. and Wilson et al., this issue, and Ref. 1.

By charter, EDF staff maintain a working knowledge of modern engineering, design, fabrication, and testing methods to serve as the Laboratory's principal resource for manufactured hardware. This expertise is a key element in APL's ability to transfer technical hardware knowledge to industrial partners. Particularly notable successes in this area have been the Transit[2] and Aegis[3]

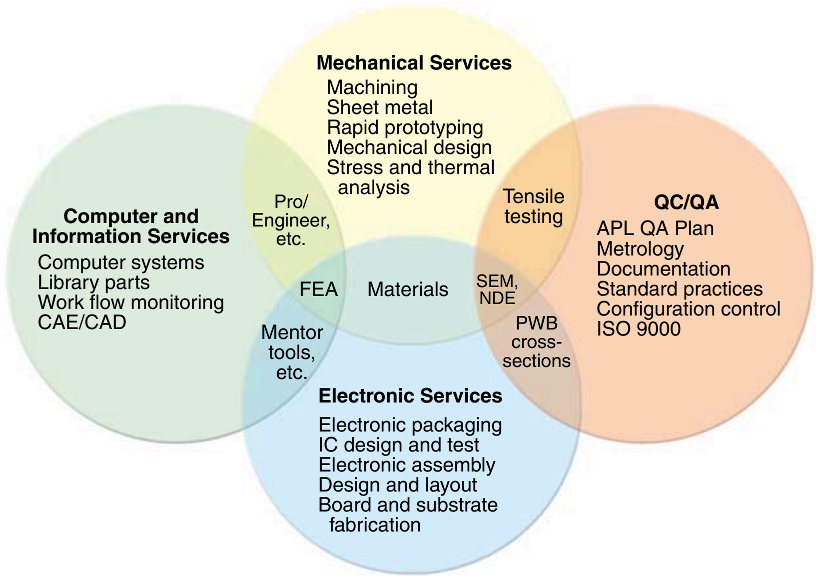

Figure 1. Major EDF capabilities and services. The overlapping regions indicate the close relationship and integrated nature of the entire spectrum of activities performed by the facility. (CAE = computer-aided engineering, CAD = computer-aided design, FEA = finite-element analysis, IC = integrated circuit, NDE = nondestructive evaluation, PWB = printed wiring board, QA = quality assurance, QC = quality control, SEM = scanning electron microscopy.)

programs, as well as several biomedical device development efforts, including an ingestible thermal monitoring pill[4] used by Senator John Glenn in his 1998 space flight. Similarly, because of its expertise in industrial practices, EDF facilitates the transfer of industrial methods to APL's government sponsors and has been called upon on occasion to rescue outside designs and fabricated products that do not meet APL or government requirements.

Support of a given program or project begins when a potential customer (either internal or external) meets with an EDF staff member to discuss a hardware product or service. Each staff member (more than 130) is familiar with all EDF service and product areas and can direct the customer to the appropriate group or person for further assistance. Each group in the EDF has a work flow administrator as well as essential engineering professionals who can help customers define their requirements in relationship to the services offered. At this stage, EDF staff can also provide a preliminary assessment of task complexity, initial cost, and schedule to the prospective client.

The EDF operates on a direct charge basis (like the rest of the Laboratory) that bills the customer for the direct labor charges, materials, and facility overhead. The EDF overhead rate is comparable to those around the Laboratory, running in the 90 to 100% range, depending on the yearly business base. Special materials and supplies that are charged directly to the customer's account are billed at cost. (References 1 and 5 contain further details on doing business with the EDF.)

When the requirements of our customers exceed EDF's capacity/capabilities, staff members can help them obtain services through off-site blanket contracts with trusted, high-quality suppliers (design, board fabrication, machining, plating, and others) or by directing them to other experts or resources. By providing this service, the EDF is able to save APL clients needed time and effort in developing their hardware applications.

EDF (and its predecessor organizations[6,7]) has supplied many thousands of hours of service a year for more than three decades. Our projects range from simple repairs, parts fabrication, and assembly involving a few hours to major projects entailing tens to hundreds of thousands of hours (Fig. 2). Examples of recent major projects include NEAR[8] (≈106,000 h or 725 staff months) and TIMED[9] (≈150,000 h or 1026 staff months).

Except for extremely small projects, which are usually handled by a particular EDF group or involve only a few people, projects ordinarily call on multiple EDF resources that transcend group boundaries and use the full gamut of the facility's services (Fig. 1). A typical project will comprise several key elements: engineering, design, and analysis support; package engineering and layout design; electrical and mechanical fabrication; electronic and physical testing; and quality control and assurance (including work flow tracking, ISO 9000 compliance, and equipment calibration). Each of these service elements is described in the following sections, which include examples from current and past EDF projects. We emphasize not only the products and services provided, but also the project planning, estimation, and work flow tracking support available in the EDF, along with developments and improvements made possible by APL funding through the Technical Facilities Pool.

ENGINEERING, DESIGN, AND ANALYSIS SUPPORT

The full range of EDF engineering development, design, and analysis services encompasses electrical, mechanical, materials, and chemical engineering. Our electrical engineers have participated in all major APL electronic system development projects, including digital, analog, and microwave electronics. A current example of our electrical engineering expertise

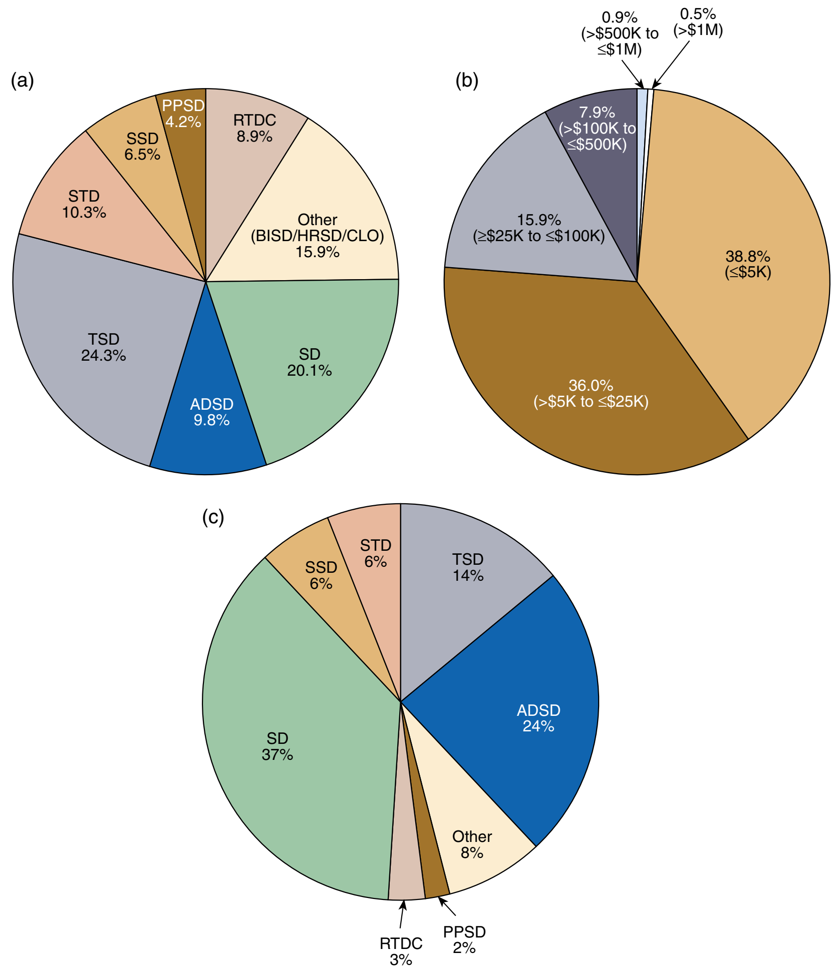

Figure 2. Distribution of customer-supported work for FY99 in the EDF. (a) Percentage of projects by department. (b) Percentage of projects by dollar value. (Note that almost 75% of EDF's projects are at the $25,000 level or less.) (c) Percentage of dollar expenditures by department. (APL department designations: ADSD = Air Defense Systems, BISD = Business and Information Services, CLO = Director's Office, HRSD = Human Resources and Services, PPSD = Power Projection Systems, RTDC = Research and Technology Development, SD = Space, SSD = Strategic Systems, STD = Submarine Technology, TSD = Technical Services.)

(Fig. 3) is the Digital Multibeam Steering (DIMUS) chip, a custom-designed integrated circuit (IC) for a digital multibeam sonar beamformer (steering element).[10] This chip contains approximately 2 million transistors and is about 3.5 cm^2. A DIMUS chip, when integrated with nine others on a single printed wiring board (PWB), replaces an entire floor-standing rack of electronic equipment in APL's Trident Sonar Processor Analyzer (TSPAN) System.[11]

Figure 4 illustrates our thin film multilayer technology. This high-density substrate technology uses a silicon carrier coated with multiple layers of copper metallization (with chromium adhesion layers) and polyimide interlayer dielectrics. The technology is capable of trace densities[12] approaching 200 cm/cm^2. At these densities approximately 1 mile of circuit track could be placed in a 25×25 cm space. Thin film multilayer technology has been used to package some of the densest APL-produced circuitry to date. The role of such dense, high chip count modules, called multichip modules (MCMs),[13] is expected to increase.

Building MCMs, because of their large population of densely placed chips, requires a great emphasis on chip reliability to ensure module yield. Figure 5 presents the yield of an MCM containing two different chip types (Type 1 and Type 2) as a function of the known good die (KGD) probabilities.[14] Here, module total cost is compared for the "no repair" case and a "single repair" with increasing complexity. It is clear from the sequence shown that repair capability is key to improving the yield and lowering the cost of high-density MCMs. The EDF has developed several repair methodologies for its MCM technology. Besides these thin film deposited MCMs (MCM-D), others, e.g., MCM-Cs (ceramic-based) and MCM-Ls (laminate-based), have been described elsewhere.[15]

In addition to the ingestible pill[4] noted earlier, our engineers have supported several other APL biomedical initiatives, including an infrared sensing system for the blind (IRIIS[16]), a virtual reality goggle projection system for the Johns Hopkins Medical Institution and Honda Motor Company, advanced three-dimensional bone modeling to study osteoporosis and injury, intravascular magnetic resonance imaging coils,[17] and a dual-energy X-ray densitometer[18] to measure bone and muscle loss in space. For these efforts, EDF personnel have performed a full range of engineering development and design services along with fabrication and system evaluation. Other EDF engineering activities have provided design and analysis for advanced APL projects such as the Cryogenic Crossbar Switch,[19] chip-on-board (COB) packaging,[20] the palm-sized Command and Data Handling System,[20] etc.

Electrical simulation models and thermal (temperature) and associated thermomechanical (stress/strain) models are fundamental to the development of advanced electronic and mechanical systems for space, underwater, and biomedical applications. A typical electrical simulation model (SPICE Equivalent) and its

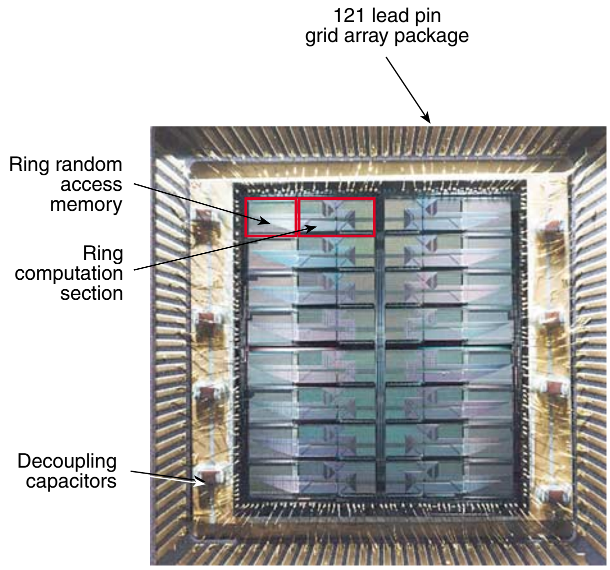

Figure 3. DIMUS IC chip custom-designed in the EDF. DIMUS uses CMOS technology and was designed with APL's MAGIC, IRSIM, and ModelSim software and fabricated through the MOSIS network. It contains 2 million transistors and uses 0.8-μm design rules.

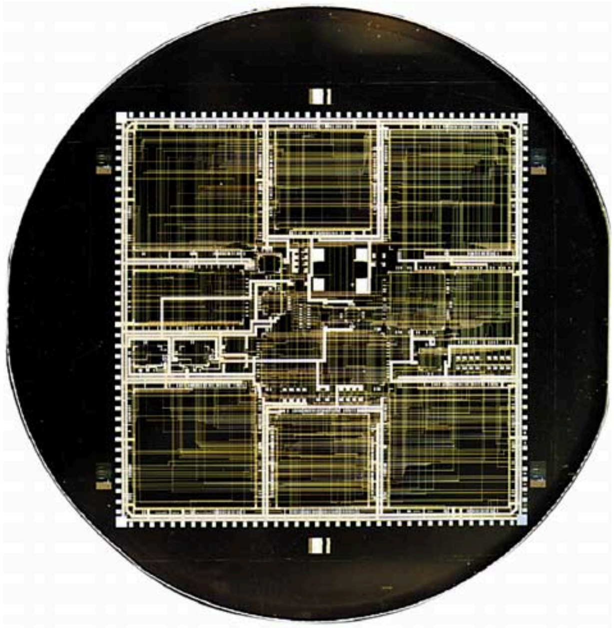

Figure 4. Thin film multilayer MCM. The substrate was fabricated using EDF's copper/polyimide MCM-D technology. It is about 13 cm^2 and contains three buried layers of circuitry. The assembled unit has 16 chips and over 1200 wirebonds.

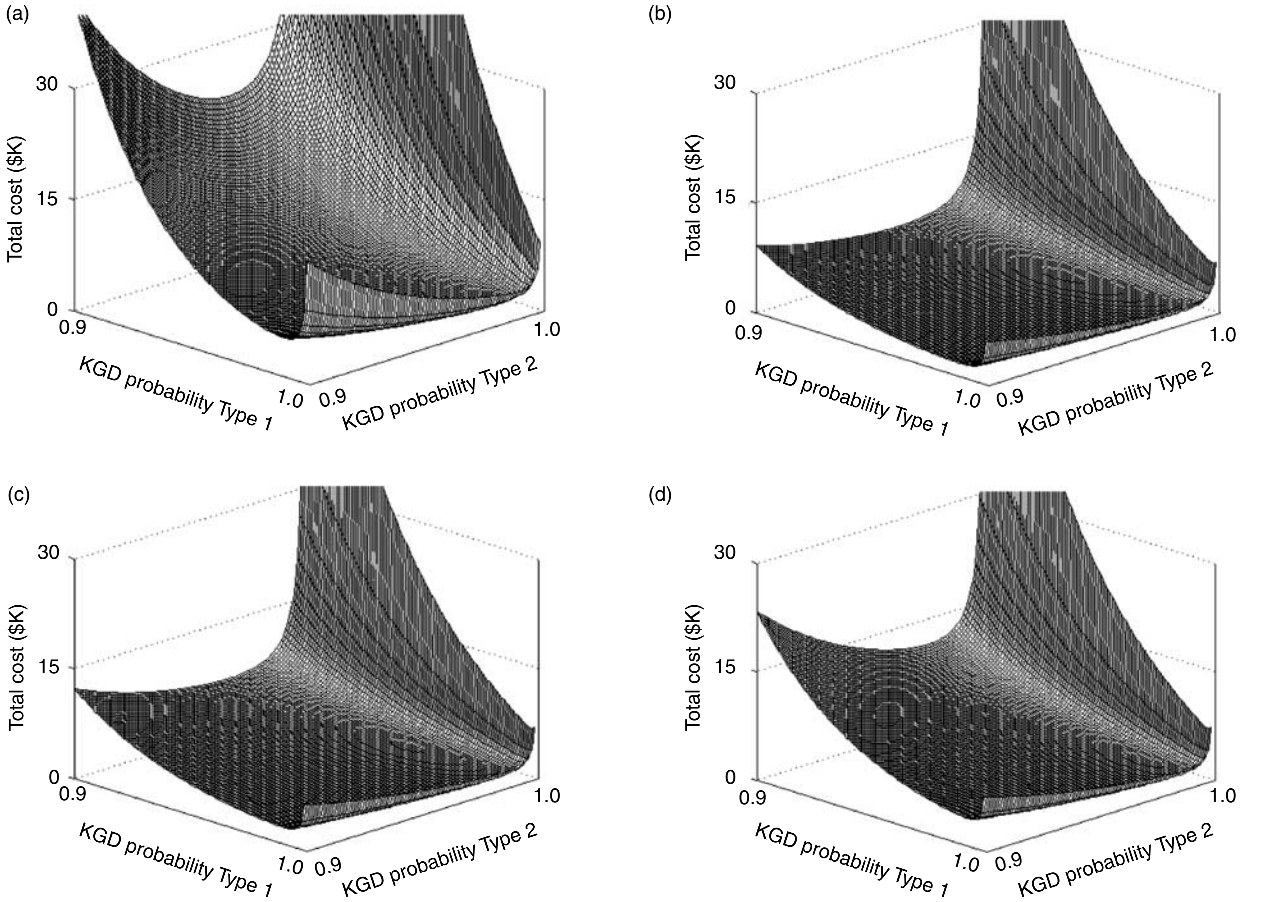

Figure 5. MCM cost as a function of known good die (KGD) for a dual-chip population under conditions of no repair (a) and single repair of low (b), medium (c), and high (d) complexity.

results are shown in Fig. 6. Figure 7 shows thermal contours and vibration amplitude for the Global Positioning System (GPS) Full Signal Translator Module circuit board due to temperature increases of the individual components. The EDF's thermal stress analysis capability has furnished design and fabrication guidelines for a wide range of electronic, electromechanical, and mechanical hardware. Figure 8 presents the results of a finite-element analysis performed on a TIMED spacecraft packaging component.

PACKAGE ENGINEERING AND LAYOUT DESIGN

The EDF has a long history of providing innovative package design and detailed layout support for a variety of APL programs. Our packaging engineers and layout designers use modern, advanced engineering workstations coupled with specialized software tools to yield the drawings and electronic files necessary to drive automated manufacturing equipment

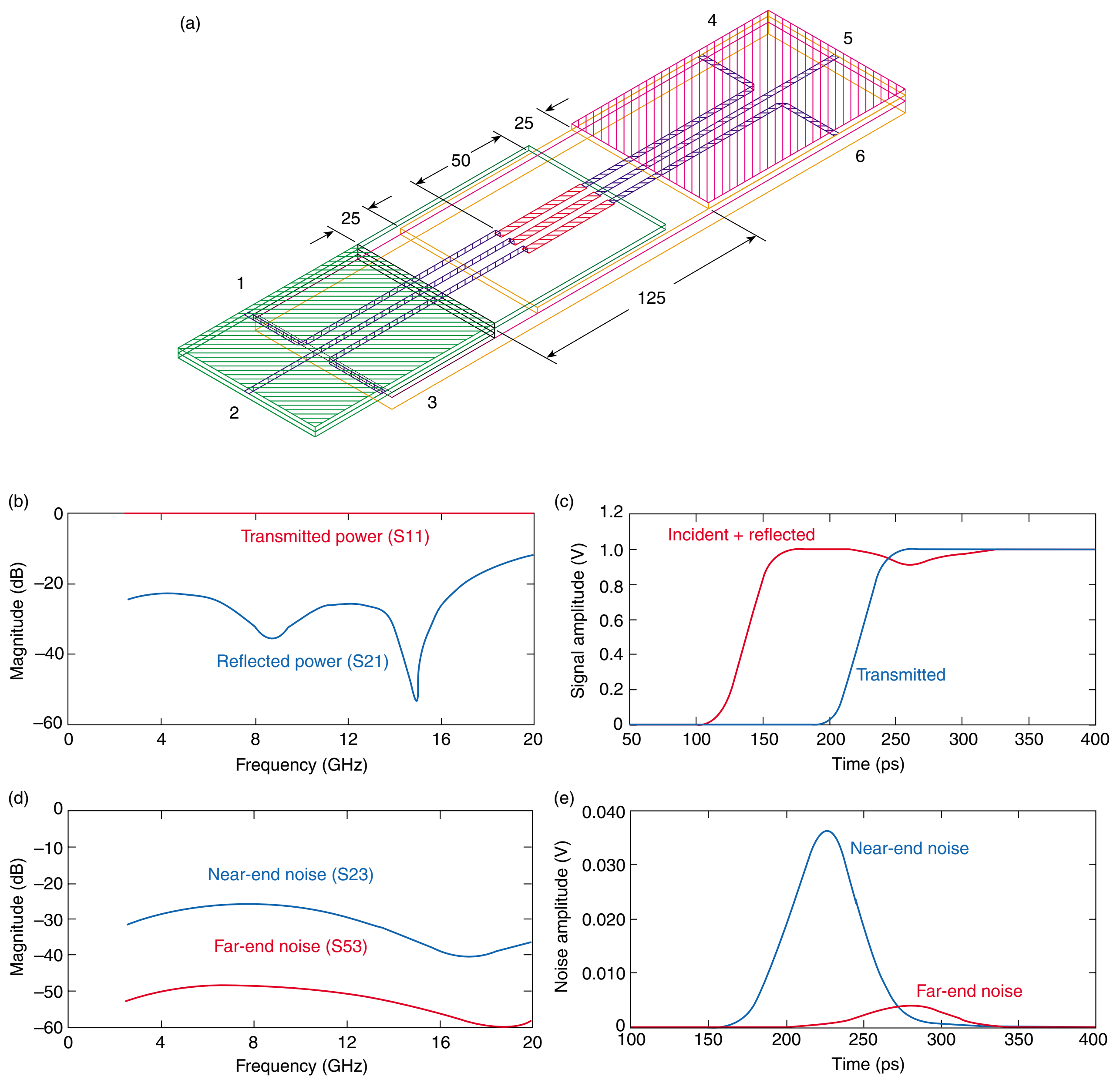

Figure 6. High-speed stripline cables to MCM-soldered interconnection. (a) Physical layout (dimensions in mils; ports labeled 1 to 6). (b) S-parameter data for cable to MCM-soldered interconnection. (c) Signal transmission/reflection analysis (9% reflected noise). (d) Cross-talk analysis S-parameter data for coupled three-line model for cable to MCM-soldered interconnection. (e) Cross-talk noise analysis (3.7% near-end noise, <1% far-end noise).

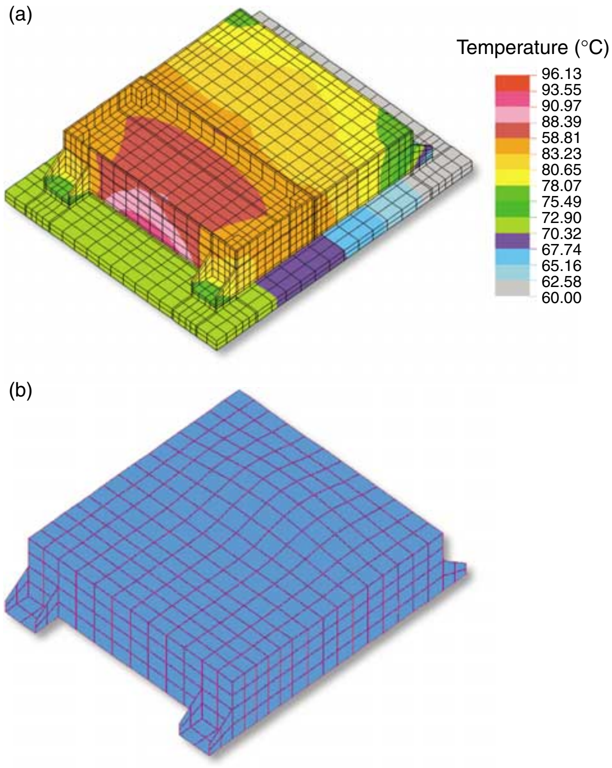

Figure 7. Analysis of the GPS Full Signal Translator Module chassis. (a) Constant temperature (isothermal) contours. (b) Dominant vibrational mode.

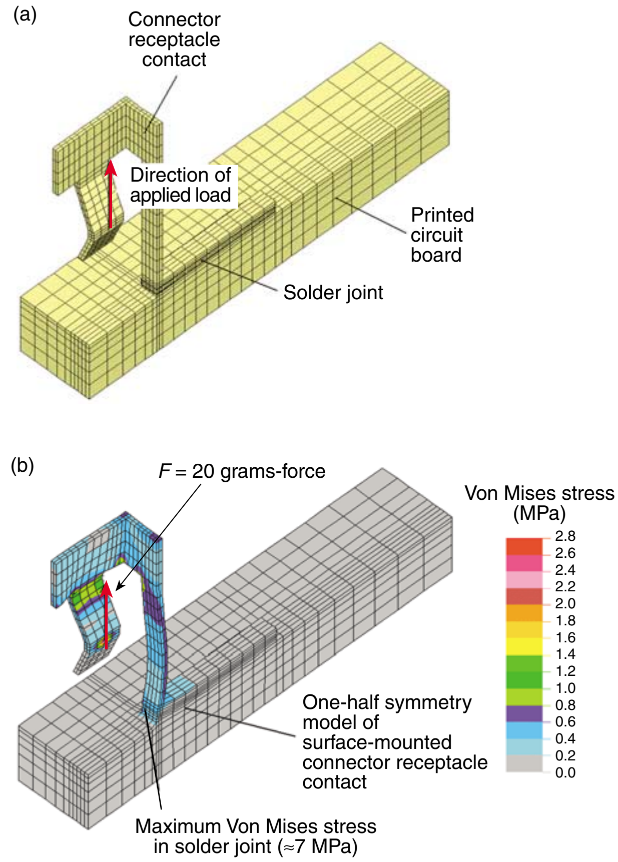

Figure 8. Finite-element analysis of a Minitek surface-mount connector used on the TIMED spacecraft. (a) One-half symmetry finite-element model of a single Minitek surface-mount receptacle contact. (b) Von Mises stress contours for the Minitek connector.

(photoplotters, board testers, numerically controlled machine tools, etc.).

The EDF provides APL electrical engineers with a diverse set of design automation tools for use with COB, MCMs, application-specific ICs (ASICs), field-programmable gate arrays (FPGAs), and PWBs. Most of these tools are supplied by Mentor Graphics and can support both traditional schematic capture and the more recent hardware descriptive language (HDL) approach to design creation. The schematic entry method still accounts for almost 100% of the PWB design work, although APL engineers have begun to embrace HDL for their FPGA and ASIC designs.

An important aspect of any computer-aided design is the ability to simulate the functionality and timing of a design *before* building the hardware. We performed the service, for each of the circuit application types mentioned, with Mentor Graphics Software tools (AccuSim, QuickSim, ModelSim, H-Spice, and Continuum). These tools not only provide specific simulators for homogeneous applications (e.g., all analog, all digital, etc.), but can also be combined on a single design using the Continuum Back Plane Mixed Signal Simulation kernel, thereby simultaneously simulating a mixed analog, digital, and HDL design.

Key to the effective use of design automation tools at APL is a standardized parts library. The EDF now has over 10,000 parts in its Mentor library. Each part defined in the library contains our in-house design rules for fabrication and assembly, and includes a schematic symbol and board geometry. The library covers a wide variety of part types, including specific ASIC library elements that can be directly linked to the MOSIS foundries through Mentor's Higher Education Program. As circuit designs embrace the latest in IC technology, the EDF will continue to maintain the library and build new library parts as an important service to the Laboratory's engineering community.

Access to the library is gained through a simple menu structure. The library is divided by circuit function, i.e., resistors are in the resistor menu, ICs in the IC menu, etc. In addition, the EDF provides simulation models for many of the library parts. Through an annual subscription contract, we can access (in addition to our own models) over 13,000 digital simulation models. We also make a Mentor Graphics analog simulation library available for customer use.

Recently, the EDF has acquired a microelectromechanical systems (MEMS)[21] software package developed by Mentor Graphics. This allows direct support of the Laboratory's MEMS efforts and provides a smooth interface with the Defense Advanced Research Projects Agency–subsidized MEMS foundry at the Microelectronics Center of North Carolina. The package includes a component library consisting of simulation models and layout generators for inertial sensors, actuators, optical devices, radio-frequency devices (RF-MEMS), display devices, and test structures.

The EDF maintains an on-site environmentally controlled Class A Halon-protected drawing vault that contains tens of thousands of engineering drawings dating back to the 1970s. In addition to paper drawings, we have tape archives, i.e., CAE system backups and aperture cards (microfilm-like copies of each drawing), for each design. Hand-drawn and/or written forms such as drawing change notices are scanned and added to the archives along with the drawings they reference.

Since 1994, we have accomplished the online archival storage (and retrieval) of design information and databases using a product data management (PDM) tool. The PDM product currently being used is Metaphase by SDRC. It contains data for over 11,000 drawings and over 1700 drawing change notices and engineering change requests. The data are available by accessing a CD-ROM jukebox that now holds 34 CDs with over 13 GB of data. The PDM has been configured to facilitate the drawing sign-off/approval for all drawing configuration levels (1, 2a, 2, and 3). The PDM product resides on an HP UNIX server and has an Oracle database engine. Over 40 users (mostly engineers and designers) routinely access the PDM either directly from a UNIX workstation or from a PC running an X-server package. PDM users can acquire report data via an APL internal Web browser. Drawings and other graphical attachments are in HDGL or TIFF format and can be viewed with a readily available plug-in.

The EDF has a documented system for the rapid prototyping of PWBs. Depending on design complexity, as determined by component density and number of board layers, different software tools are used in the rapid prototyping process. Pantheon Intercept software is used to create parts and perform the layout and routing of simple-to-medium complexity designs. Mentor tools are used for more complex designs. A well-defined path through design, fabrication, and assembly has been established to provide contingencies for delays at any step. The process has been employed successfully on several Level 1 designs. Typical turnaround times have been on the order of 1 week.

On the mechanical side, the major piece of design software is Pro/Engineer developed by Parametric Technologies, Inc. Pro/E, as it is commonly called, is an interactive tool based on parametric design methods. For example, instead of indicating the dimensions of a box as 10 cm in length (l), 5 cm in width (w), and 150 cm in height (h), the box dimensions are described as an analytic expression (e.g., lwh). The expression can be composed of independent variables (such as l, w, or h), or one or more of the variables can be dependent on other variables being used to define the measurements of other objects in the design (e.g., the box length is equal to twice its width). This parametric approach results in an increased emphasis on the creation of a model of the design rather than a drawing of the design. The drawings are then simply the output products of the model. Until the model or parametric relationships are changed, the model remains invariant under scaling. Thus, a change in an input (independent) dimension will change the output drawings to reflect the dimensional change, but the model will remain the same.

Pro/E can check for interference and can also calculate the weight (based on the density of the constituent materials) and center of gravity of the set of objects comprising a design. A clipping feature allows a model to be cross-sectioned at any depth, which enables the engineer or designer to better understand the relationships of objects within the design. In addition to drawings, Pro/E is capable of outputing databases that can be used directly by EDF's numerically controlled machine tools. This allows for the unattended fabrication of intricate mechanical parts, composite-resin rapid prototypes, and complex sheet metal assemblies.

ELECTRICAL AND MECHANICAL FABRICATION

EDF's electrical and electronic fabrication facilities are located in Building 13 (the Steven Muller Center for Advanced Technology). They include our certified PWB fabrication line (certified to MIL-PRF-55110F and MIL-P-50884, Type 3 (GI Material) and Type 4 (adhesiveless)) and Class 1,000 clean rooms[22] used to fabricate and assemble microelectronic devices and modules such as the large, multilayer, high-density PWB produced for the TRIAGE Program shown in Fig. 9. The MCM substrate shown in Fig. 4 is a recent example of our microelectronic activity.

Recent EDF work on fine-line boards with blind and staggered vias for COB applications[20] is illustrated in Fig. 10. COB can potentially miniaturize APL systems by a factor of 10 to 100. Examples of a COB implementation of a standard spacecraft electronics box are shown in Fig. 11. Essential to making the COB process work was EDF's development of a neutral pH autocatalytic gold plating solution, along with associated processing methods.[23]

Other advanced board development efforts have involved the use of electro-optic–sensitive polymers such as the dielectric layers in MCMs. These layers can be probed nondestructively using a laser. Laser mapping of the electric fields within the dielectric layers adjacent to

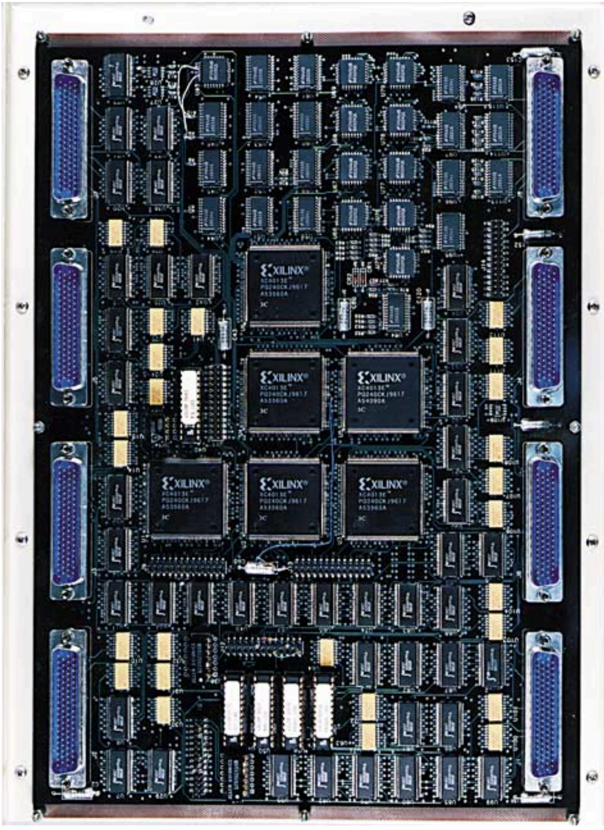

Figure 9. High-density PWB developed for the TRIAGE Program. This radar data collection board contains 10 circuit layers, 4883 vias, and 422 components, with 6052 internal component connections and 624 input/output pins. This single board replaced the five boards used in a previous system.

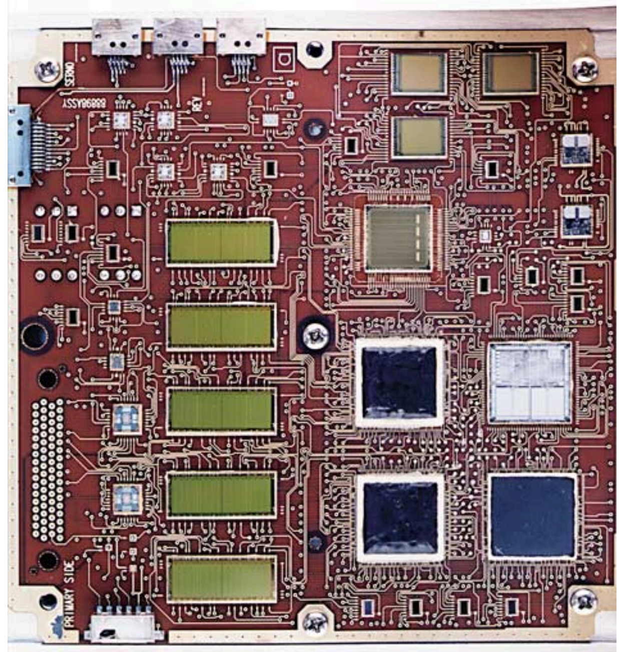

Figure 10. COB substrate containing blind and staggered vias. This 12.3 × 12.3 cm board is being used for the palm-sized Command and Data Handling System.[19]

device structures of interest can be made. This APL invention offers great promise for testing complex electronic structures.[24] The polymer material is made electro-optic by doping and selective poling (application of a strong electric field while material is cured). Thus, regions of doped and unpoled material can be made adjacent to doped and poled material. As there is an index change in the doped material upon poling, integral light guides can be made selectively in the dielectric layers. These APL-developed techniques,[25] therefore, offer the potential for integral light guides in MCM dielectrics along with the ability to nondestructively evaluate module performance.

In addition to advanced-performance circuits and boards for high-reliability spaceflight use, EDF's electronic fabrication facilities create a large volume of more conventional electronics. These are intended for ground and shipboard use and support myriad one-of-a-kind experiments conducted by our scientists and engineers, both at the Laboratory and off-site.

Mechanical fabrication is performed with advanced machine tool equipment located in Buildings 14, 39, and 41. This equipment includes computer-numerically-controlled (CNC) lathes, mills, turning centers, and sheet metal punches. Three CNC electrical discharge machine tools, plus both carbon dioxide[26] and Nd:YAG lasers (in Bldg. 13), are the heart of EDF's advanced contactless machining activity.

Figure 11. COB implementation of the NEAR Command/Telemetry Processor (24 × 24 × 17 cm, 5 kg) compared with the palm-sized Command and Data Handling System (11 × 11 × 5 cm, 0.5 kg).

A computer-controlled rapid prototype machine is also available. It is capable of making realistic (dimensionally accurate) three-dimensional polymer replicas from files downloaded from our CAE systems. Examples of rapid prototype–produced replicas are shown in Fig. 12. EDF's organic composite fabrication activities are housed in Building 14. Further description of our composite work is given by Wilson et al., this issue.

Fabrication involves more than just the manufacture of advanced electrical and mechanical parts and systems. It also involves the application of the tools normally associated with hardware fabrication to support other aspects of APL's scientific and engineering activities. For example, EDF's photolithographic resources have been used to pattern gratings for optical experiments, sensors for biomedical and ocean physics applications, and thin films for basic research. Our carbon dioxide laser machine tool[26] has been employed in material ablation studies and for novel pattern generation in unconventional materials. It has also served as a heat source for material alloying. The rapid prototyping system has been used to fabricate real parts (not just models or replicas) in short-duration experimental situations. Such innovative use of standard production tools, necessary for APL's and EDF's mainstream hardware production, gives APL a flexible resource to augment its research facilities in other parts of the Laboratory.

Our expertise in the fabrication of hardware is a chief element that distinguishes the Laboratory from many other research and development centers. This hands-on hardware development resource of the EDF helps form APL's internationally known systems engineering capability.

ELECTRONIC AND PHYSICAL EVALUATION

The EDF offers a wide range of electronic and physical testing services. Our electronic test equipment can perform exacting electrical tests for analog, digital, and microwave circuits. Components and circuits can be tested from DC to 50 GHz. This allows us to verify manufacturers' published data sheets, provide device and subsystem data not available from manufacturers, and evaluate "edge-of-the-envelope" parameters when commercial-grade parts are pushed beyond their published limits. Tools and expertise in the EDF enable us to execute extensive DC parametric tests on devices. For example, leakage current values can be validated or the variation of leakage current with respect to supply voltage can be measured. In addition, transistor characteristic curves can be generated for all device types (bipolars, field-effect transistors, power transistors, hetero junction bipolar transistors, etc.).

We can also perform AC characterization of components of frequencies from a few millihertz to 50 GHz using vector network analyzers. Spectral analysis capability up to 26.5 GHz is currently available, with plans to upgrade to 50 GHz. These measurements are used to characterize passive and active circuit components, subsystems, and materials for frequency, time, phase, and noise parameters. The EDF specializes in the design and fabrication of custom test fixtures and the use of automated testing equipment and methods to greatly speed the testing process and eliminate operator biases and errors. Over the last few years, these methods have been used on a variety of APL programs, including CASSINI, MSX, NEAR, ACE, and TIMED.

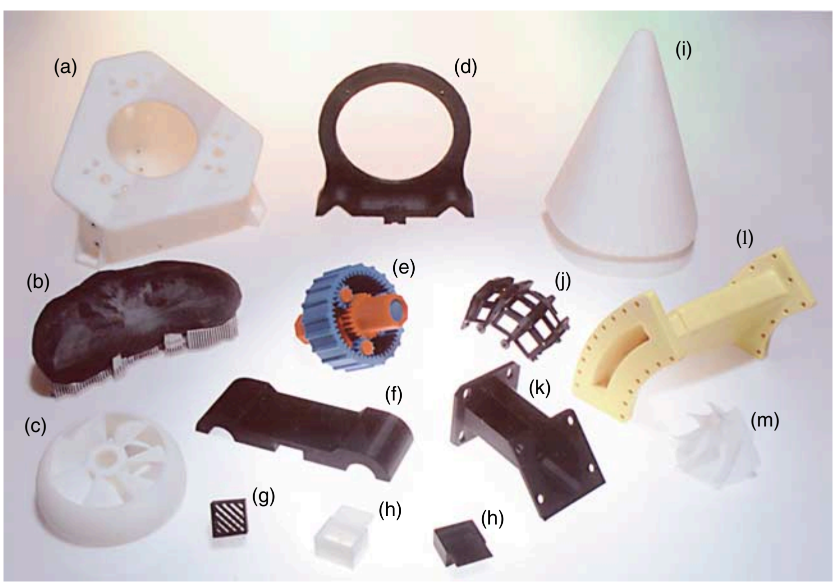

Figure 12. Rapid prototype replicas produced by an EDF automated polymer casting machine. (a) TIMED Doppler Interferometer telescope mount. (b) Model of 443 Eros asteroid. (c) Impeller thruster. (d) Speaker-mount for Primate Vocalization Program. (e) Planetary gear. (f) Clamp for Primate Vocalization Program. (g) Gridded array. (h) Transmitter boxes for Primate Vocalization Program. (i) SCAMP pod faring. (j) Video display chip mount/virtual reality helmet. (k) TIMED solar array bracket. (l) Mach 6 supersonic nozzle for dual-combustor ramjet. (m) Impeller.

Virtually every electronic device—whether a printed circuit assembly, an MCM, or a custom IC—involves a substrate onto which one or more components are attached. This substrate contains conductive traces that interconnect the device to other circuit elements on the board as well as interface it with power supplies and adjacent modules in the system. Depending on the application and design, the substrate will take many forms. It may be a multilayer printed circuit assembly with internal traces and interconnecting vias of plated copper, a 1-μm-thick thin film of aluminum or gold on a silicon wafer, silk-screened patterns of conductive traces and resistors on a ceramic substrate, or many other alternatives.

With today's demand for smaller devices, higher frequencies, and tighter specifications, many of the fabrication techniques used to create the circuit elements on the substrate are being pushed to their limits. The substrate must therefore be tested to ensure that conductors are not inadvertently shorted to each other and are continuous between the elements being connected. Elimination of the patterned substrate as a potential cause of failure saves time and money, as expensive parts are not assembled onto a substrate that is found to have incorrect or defective circuitry.

The BSL LinearProbe II Tester in the EDF has been employed for the past 5 years to perform 100% testing of all substrates used in the assembly of electronic devices. This fixtureless flying probe system is designed to test either bare or populated substrates. In 1998, over 800 printed circuit boards and other substrates were tested. The system simultaneously tests both sides of a substrate up to about 61 × 61 cm, regardless of the material of construction. The average double-sided printed circuit board takes less than an hour to test, including initial machine setup and CAE file compilation.

The tester evaluates all circuitry networks ("nets") for opens and shorts. Testing for opens is accomplished using a standard four-wire resistance measurement. Testing for shorts uses a capacitance measurement for test node reduction, and then resistance for verification of the suspect shorts; another option is to compare measured net resistance to a predetermined standard. The tester can be configured with a variety of probe types (size and alloy) depending on the pad size and material. Probes as small as 45 μm in diameter are available, permitting contacting to pads as small as 90 μm in width. Probe location is repeatable to ±5 μm. Depending on which probes are used, up to 20 tests per second can be performed.

The BSL tester can interpret a variety of CAE database formats to determine where to probe each net. The CAE file supplies the necessary location, nomenclature, and net information to the tester. If no database is available, the tester can be manually "taught" where the testing points are located. In either case, it can sequentially test up to four identical substrates on a common panel. The tester can also be used to test for net-to-net isolation breakdown by applying a high voltage between adjacent traces and monitoring for current flow.

In addition to electronic equipment, the EDF maintains and operates a complete range of physical test and failure analysis equipment to support our internal hardware fabrication and to provide physical testing services to our customers. Physical testing includes mechanical stress/strain, hardness, and metallurgical microstructural analysis along with a suite of nondestructive evaluation tools (e.g., several methods of ultrasound evaluation, acoustic microscopy, and eddy current testing).

A full array of advanced material and chemical evaluation tools also exists within the EDF. Such tools as a scanning electron microscope, energy dispersive X-ray analyzer, Fourier transform infrared spectrometer, inductively coupled plasma spectrograph, and tabletop secondary ion mass spectrometer are routinely used in support of efforts for TSD, Laboratory programs, and sponsors. For example, in the Standard Missile Program, the protective nickel plating on the copper case of a high-power electronic switch was found to be peeling from a large percentage of devices. Since the missile manufacturer had only one vendor for this specialized device, missile production was threatened. Because of its varied imaging capabilities and detectors, the scanning electron microscope proved to be an ideal tool for diagnosing the problem. Upon optical microscope inspection, the copper exposed by the peeling did not appear to differ greatly from surfaces in which the nickel layers had been poorly adhered to the copper during the plating operation. However, energy dispersive X-ray (Fig. 13a) and Robinson backscattered electron imaging (Fig. 13b) analysis of the blistered area showed silver beneath the nickel.

An investigation of the processes used to fabricate the device indicated that the package had electrical feed-throughs brazed to the copper case before plating. The presence and distribution of the silver showed that the copper/silver brazing alloy had wicked along small grooves that were introduced into the surface during the machining of the case. The chemical baths used to clean the packages prior to nickel plating had been selected with the assumption that the surfaces were only copper, with no silver present. The silver left on the surface from the brazing operation had reacted with the ambient air to form compounds that were not removed during the cleaning process. Thus, a thin layer of contaminant was present during the nickel plating process, and the deposited nickel could not atomically bond to the copper surface. With this input, the vendor was able to improve his process and deliver acceptable parts.

QUALITY CONTROL AND ASSURANCE

Inspection

The EDF maintains a fully staffed and equipped quality assurance capability. Our materials analysis and quality assurance facilities offer customers many

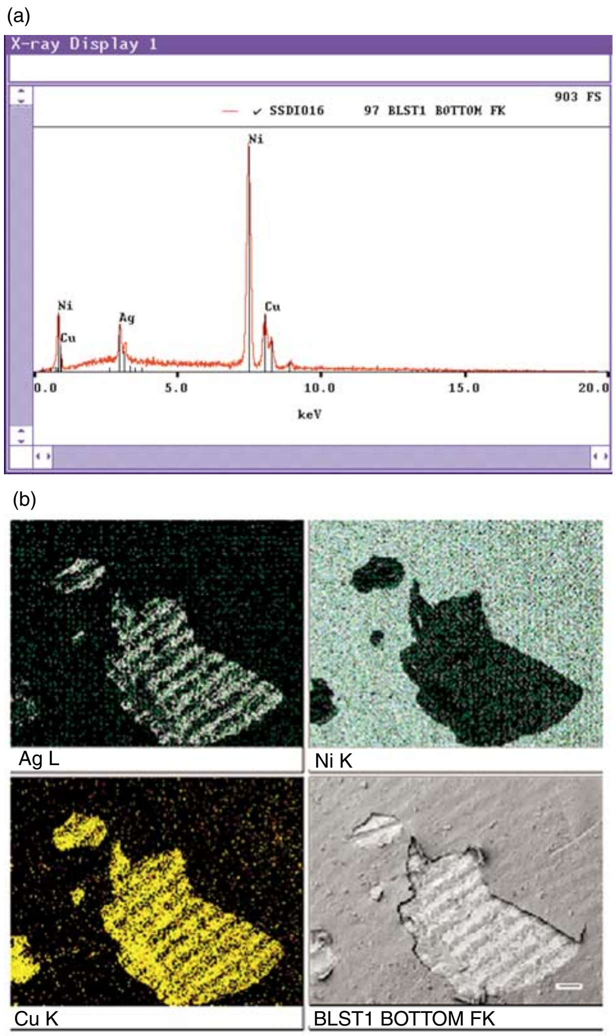

Figure 13. Energy-dispersive X-ray spectrum (a) and dot maps (b) of a blister on the nickel-coated copper case of a high-powered electronic switch. Dot maps shown are for silver, nickel, copper, and a scanning electron micrograph of the region.

inspection, configuration control, documentation control, storage, and parts kitting (preparation of assembly kits) operations. These services are central to our ability to ensure that our customers' quality assurance requirements are met. Major documents controlling EDF activities in this area—the Laboratory's *Quality Assurance Plan*,[27] *Hardware Configuration Management Manual*,[5] *Electromechanical Hardware Workmanship Standards Manual*,[28] and nearly 200 standard processes and procedures[29]—set standards and directions for our operations. As part of EDF's quality assurance practice, staff are trained and certified in many skill areas. For example, the EDF operates and maintains a fully certified NASA solderer training program.[30] Every 2 years, approximately 30 Laboratory employees are certified to solder or inspect to NASA standards.

Electrical and mechanical inspection of hardware are both routinely performed. For the former, inspection starts at the design level, where schematics, net lists, and board layouts are compared for accuracy and compatibility using sophisticated checking software. Manufacturing design rule checking is automatically done at the panelization or presubstrate fabrication step. After fabrication, boards are visually inspected and then electrically tested using our BSL tester. Upon assembly, boards are inspected to print for component placement and workmanship. Electrical verification at the board level helps ensure the integrity of the assembled product.

The EDF has developed many other services to support customer and Laboratory quality assurance requirements. These include precision mechanical measurements using computer-controlled coordinate measurement machines to ensure that fabricated parts meet specified dimensions and tolerances. The EDF has been a leader at APL in standardizing mechanical design methodology to allow the rapid electronic capture of design files from both internal customers and outside organization. Our use of geometric dimensioning and tolerancing[31] to permit the widest possible allowed tolerances has made APL drawings directly usable by most industrial organizations.

The recording of measurements certifies that the individual parts meet design specifications, and those measurements form the basis of our statistical process control efforts. Out-of-tolerance conditions are entered into computer databases, sorted by root causes, and then analyzed (Pareto diagrams, etc.). Such an analysis helps identify areas for internal process improvement, additional staff training needs, machine repair (or calibration) requirements, and the need for new equipment and processes. We routinely practice statistical process control in our design, fabrication, and testing operations to ensure the quality of the process and, hence, the quality of the delivered design or fabricated parts. Examples of control charts and other statistical process methods have been discussed previously.[6]

We are always exploring other techniques to quantify the quality of our delivered products. For example, we have used mechanical (wirebond pull[32] and ball bond shear[33]) testing in conjunction with thermal aging techniques[23] to determine the integrity of microelectronic wirebonds (Fig. 14). Today, we are exploring a new laser-acoustic technique for determining bond quality.[34] In this technique, a highly focused laser source strikes the ball bond and causes a thermoelastic excitation of the bond, which induces an ultrasonic or acoustic vibration to propagate in the substrate adjacent to the bond. The surface wave portion of this acoustic signal is sensed by a laser interferometer and used to determine bond quality. An example of the acoustic signatures with time for as-made and thermally aged bonds is shown in Fig. 15a.

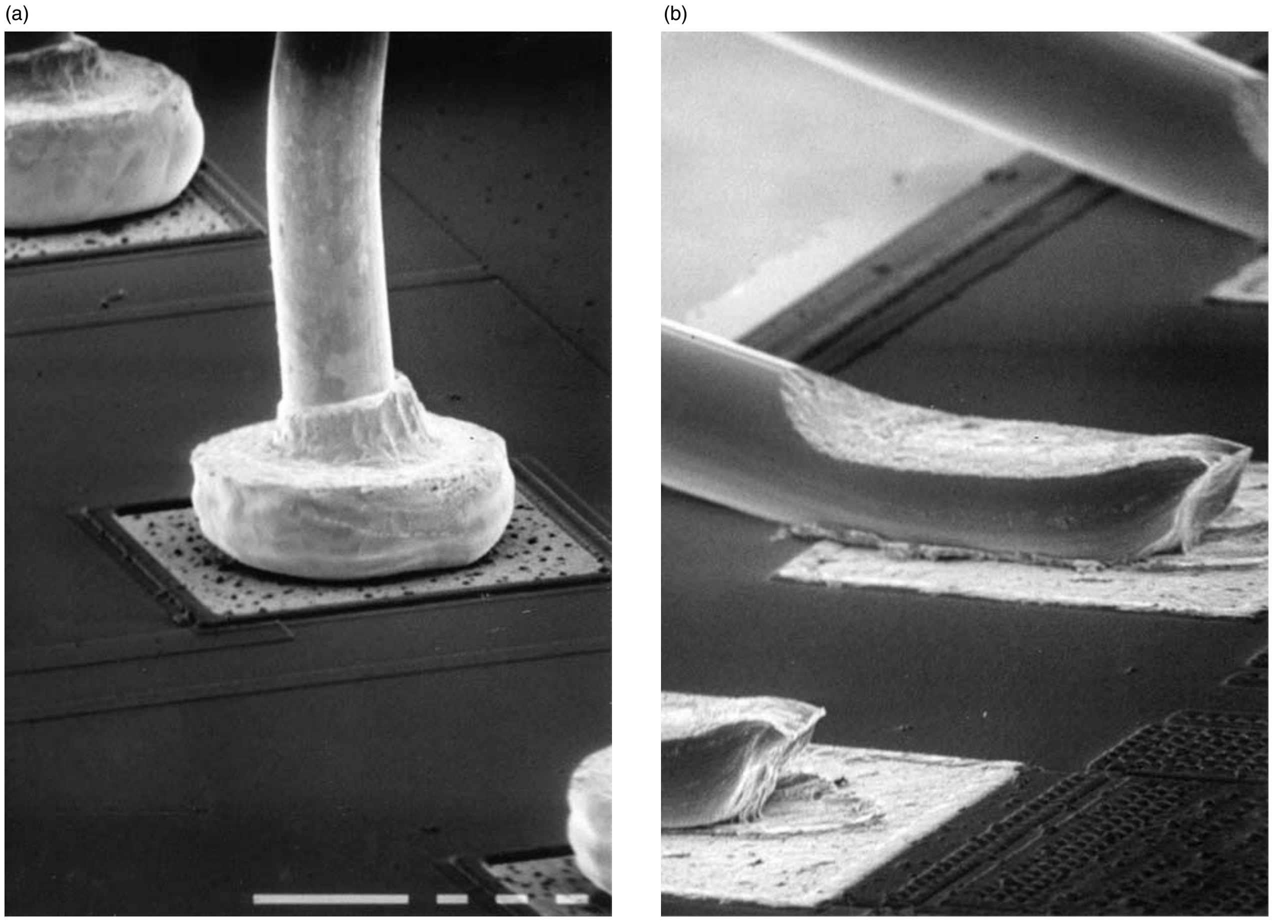

Figure 14. Microelectronic ball (a) and wedge (b) wirebonds.

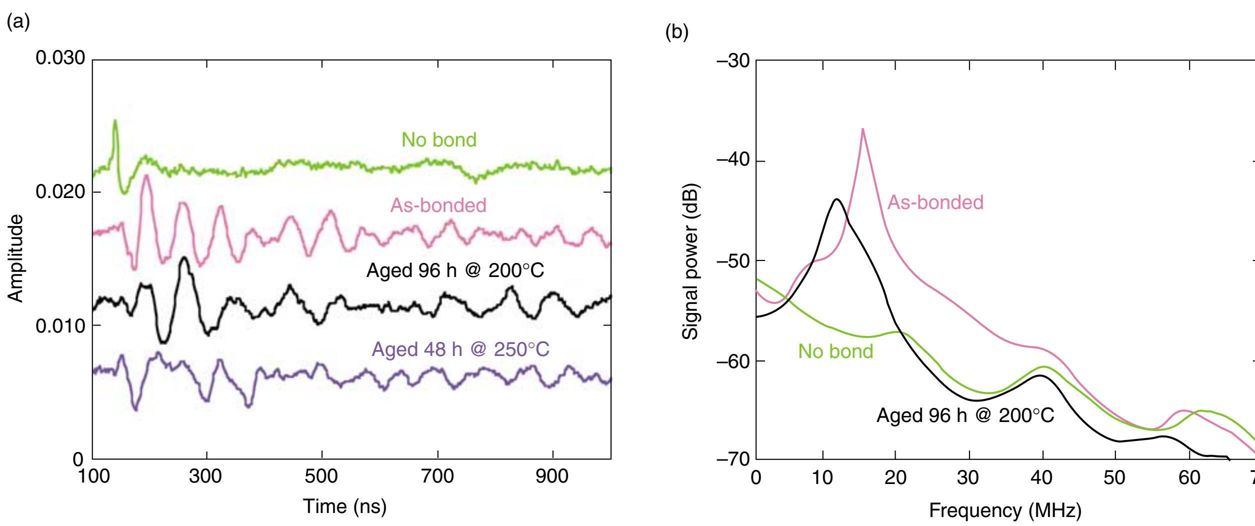

Figure 15. (a) Surface amplitude versus time as the wave train passes the silicon surface position detector as measured for differently aged samples (offset for clarity). (b) Example of the power spectral density numerically extracted from the time domain data in (a).

While obvious differences exist in the signals, it is difficult to ascribe any significance to the changes. Applying Fourier techniques as shown in Fig. 15b produces a dominate resonant peak for each sample. From our testing, it appears that as our bonds are aged, the frequency of the dominant peak diminishes in amplitude and shifts downward in frequency. Work is under way to correlate these changes with ball bond failure mechanisms such as the excessive growth of aluminum/gold intermetallics.

ISO 9001 in TSD

ISO 9000 is a set of standards for a quality assurance system developed by the International Organization for Standardization.[35] Nearly 100 countries have adopted these standards with only minor variations. From an APL/TSD perspective, the most significant component standard is ISO 9001,[36] which applies to organizations involved in the development, design, manufacture, installation, and servicing of products. To satisfy the requirements of some sponsors and improve the quality of our own internal processes, APL is working to become ISO 9001 compliant. The main proponents of this thrust are in the Space Department and TSD.

APL will be contractually required to be in compliance for many future NASA programs. On 8 June 1998, NASA's Office of Safety and Mission Assurance issued Directive NPD 8730.3, *NASA Quality Management System Policy (ISO 9000)*. This document indicates that "where appropriate and beneficial," NASA will require suppliers to comply with ISO 9000 or to be certified to ISO 9001 by third-party examiners. At this time, all major NASA facilities have been certified to ISO 9001 as required.

All impacted groups in TSD have completed an internal audit to identify areas where we did not comply with the requirements of ISO 9001. The results of this analysis were entered into a database procured specifically for tracking compliance. Those data are online and are shared with the Space Department and other cognizant activities at APL. Estimates of the time and cost required to become compliant have been prepared, and many corrective actions have been implemented already. Most of the improvements needed to comply with ISO 9001 require documentation of existing procedures for which there are no written descriptions.

One of the most significant aspects of ISO 9001 is the preparation, distribution, and control of processing instructions. The standard covers all aspects of the task of documentation, from initial sign-off to archiving. Perhaps the most difficult yet most important requirement is to ensure that only the most current version of a document is available to those performing the process described.

As noted earlier, TSD has nearly 200 fabrication standard processes and procedures[29] that describe virtually every process used in the fabrication, assembly, and testing of electronic and mechanical hardware. All of these have been converted to electronic format and are available on an internal APL Web site. Subject and title indexes are also included in the online version. These documents are retrievable from anywhere within APL.

TSD will continue to make improvements and document processes until we can be assured of ISO 9001 compliance. Hopefully, this will occur during calendar year 2000.

Work Flow Tracking

The EDF is committed to effectively tracking work progress and monitoring job costs on all of its projects. To aid in these important tasks, we have recently acquired and implemented a computerized work tracking system, VISUAL Manufacturing (VM) software from Lily Computers, a powerful tool for scheduling and estimating in a manufacturing environment. VM is a network-based management information system designed for custom and mixed-mode manufacturing, as is the norm in TSD. It utilizes a fully relational Oracle database, and data can be retrieved and analyzed in multiple ways.

Service-specific routings, coupled with master engineering flow documents, define the logical sequence of tasks to be performed. Estimates are made to reflect the effort needed to complete each step of the work. The routings and flow control documents accompany the work in the form of a "traveler" and ensure that the proper steps are performed.

Required resources, both labor and equipment, are identified for each step. Allocation and balancing of these resources across all tasks provide a means to predict the need for additional resources. Early process planning with the customer ensures that the requirements of the program over its full duration can be satisfied before beginning work.

Data are collected via terminals throughout the EDF using either a customized Web-based entry screen or automated bar coding. Material and service costs are collected and recorded for each step. Services procured external to the EDF (e.g., painting, carpentry) are also tracked and recorded. Job status and accumulated costs are available in real time and can be monitored through the APL internal Web server using preformatted reports. Full historical documentation is archived and readily available for use as a baseline to estimate future work.

As labor hours are charged against the work in progress, VM collects and compiles information relating to both schedule and financial status. Data are gathered on who performed a specific task, how much time was charged to the task, the date the task was performed, and whether a milestone was completed. These data are compared to the estimated duration and scheduling of each step to determine if the work is proceeding on time and at cost. The progress of any EDF task can be tracked as work is completed and compared with the preestablished cost estimate and schedule.

VM is applicable to any task: simple or complex, fabrication or engineering, analysis or design. Its routings are capable of providing a tree-like hierarchical structure that represents a drawing package of interrelated products. This interrelationship in the system leads to improved communications across group boundaries and ties together EDF's very diverse disciplines. With both service providers and customers having access to the same data, communication is vastly improved and customer satisfaction enhanced. This software greatly increases our capability to operate competitively by allowing TSD to respond to our customers' needs more effectively, better predict and monitor costs, and use resources more efficiently.

Metrology

During 1999, APL owned approximately 3000 pieces of electronic, physical, and dimensional test equipment categorized as Class 1. As such, they were routinely scheduled for calibration.[37] In addition, there were over 10,000 items of test and measurement equipment (T&ME) that were categorized as Class 2. Class 2 T&ME is calibrated and repaired on an as-needed basis, but receives the same level of attention.

The Metrology Office is responsible for administering the APL calibration program,[37] coordinating external and internal calibration and repair activities, and supporting those APL groups that perform special-purpose T&ME calibration and repair. The office is charged with ensuring that all Class 1 measurements are made with equipment that is traceable to standards maintained at the National Institute of Standards and Technology or to natural physical constants. In addition, the office must see to it that T&ME equipment is calibrated on a fixed schedule and that proper documentation of these calibrations and repairs is maintained.

Historical records are kept to help determine if equipment should be considered for replacement owing to being out of calibration too often. The Metrology Office provides recall and overdue information to APL Instrument Coordinators so that Class 1 items can be submitted for calibration in accordance with the published recall interval. It also provides notification to users when Class 1 equipment is found to be out of tolerance when received for calibration so that the impact on measurements and tests performed since the equipment's previous calibration can be determined.

The Metrology Office is located in Building 16 and occupies approximately 74 sq. meters. It includes a technical library, an equipment staging area, and administrative support. The office maintains a computerized calibration management system and the associated hard copy records for every calibration and repair. It also provides assistance and guidance in the calibration, repair, acquisition, operation, and interpretation of T&ME to all APL groups. The technical library includes operation and service manuals for a large segment of APL's electronic T&ME. This collection is available to all T&ME users at the Laboratory and is also occasionally used by the outside facility contracted to perform calibration and repair services.

The Metrology Office was established in 1993, when APL's Calibration Laboratory was disestablished. Since then, virtually all of the calibration and repair work has been subcontracted to outside facilities. This has resulted in an annual cost saving of approximately $400,000 when compared to the 1992 Calibration Laboratory budget. As a further means to reduce operating costs, T&ME users have been requested to continuously evaluate their equipment and to submit only those items for calibration that are used for Class 1 measurements. In this way, equipment that is no longer being used, or is not being used to make Class 1 measurements, can be reclassified as Class 2. This has allowed the annual number of calibrations performed to be reduced from 5629 in 1992 to only 2092 in 1998, a reduction of 63%.

In addition, users have disposed of, replaced, or downgraded their unstable T&ME so that out-of-tolerance items have decreased from 3.3 to 0.7%. These actions have reduced the potential for suspect data and the cost associated with Out-of-Tolerance Alerts. The Metrology Office also now sends Instrument Coordinators a mid-month notification of equipment due for calibration in the following month, which helps keep the number of overdue items down; overdue items have decreased from an average of 364 in 1994 to 42 in 1998.

The Metrology Office has also implemented a new property and calibration management software system. With this system Instrument Coordinators can access the status of calibration and repair activities as well as calibration history via the APL intranet.

SUMMARY

The EDF performs complex and dynamic electronic, electromechanical, and mechanical hardware design and fabrication services which range from initial concept development to the delivery of fully tested and qualified hardware products. Such services have been provided by the EDF and its predecessors since the Laboratory's inception.[38] The ability to design, fabricate, and test hardware in-house has always been a distinctive feature of APL, and has set it apart from similar university and government facilities. Building upon the extensive modernization and building programs of the 1980s and early 1990s, the Laboratory continues to make significant investments in the EDF. Such investments are necessary to ensure that resources for modern electronic and mechanical design and fabrication continue to be in place for APL and its sponsors during the 21st century.

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THE AUTHORS

HARRY K. CHARLES, JR., holds a B.S. and Ph.D. in electrical engineering from Drexel University and JHU, respectively. He is a member of the APL Principal Professional Staff and Assistant Department Head for Engineering in TSD. Dr. Charles has worked for over 25 years in microelectronics, specializing in electronic devices, systems, packaging, and reliability. He is a Fellow and former President of IMAPS, an IEEE Fellow, and a member of the Board of Governors of IEEE's CPMT Society. He has received international recognition for his research, development, and teaching activities, including ISHM's Technical Achievement Award (1987), Maryland's Distinguished Young Engineer (1989), JHU's Outstanding Teaching Award (1992), the CPMT Board of Governors' Outstanding Service Award (1992), ISHM's Distinguished Service Award (1994), and the IMAPS Daniel C. Hughes Memorial Award (1998). Dr. Charles has published over 160 papers on electronic devices and packaging and has received numerous awards for best papers. His e-mail address is harry.charles@jhuapl.edu.

JOEL A. WEINER received a B.S. in chemistry from Brooklyn College of the City University of New York in 1970, an M.S. in chemistry from Rutgers University in 1974, and an M.S. in technical management from JHU in 1987. Before coming to APL in 1982, he was a Research Associate at RCA's David Sarnoff Research Center, and then Director of Product Technology for Technics, Inc. Mr. Weiner is currently the Quality Assurance and Improvement Manager for TSD and a member of the APL Principal Professional Staff. He also served as Assistant Supervisor for the Microelectronics Group and the Electronic Fabrication Group. He has an extensive background in quality assurance, high-reliability electronic assembly, thin film material science, and chemical processing for semiconductor and electronic fabrication. Mr. Weiner has published or presented over 50 papers and holds 4 U.S. patents. His e-mail address is joel.weiner@jhuapl.edu.