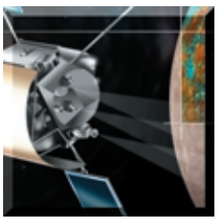

Advanced Spacecraft Technology Program

Robert E. Jenkins

Insight is given into the APL Space Department's Advanced Technology Development Program for spacecraft. After 40 years in the business of developing spacecraft, new technology and new methods entailing risk are still the lifeblood of the Laboratory's contributions to the national space program. Today's political environment concerning the use of new techniques in spacecraft and how we have come to that environment are briefly described. The underlying technical thinking behind our current efforts is presented, with an emphasis on what we are doing and why (rather than the details of how), and where these activities may lead us in the future. These efforts include scalable architectures, miniaturization, custom integrated circuits, spacecraft autonomy, and ultra-low-power electronics. (Keywords: Advanced spacecraft architectures, Spacecraft autonomy, Spacecraft miniaturization, Spacecraft technology.)

CHANGING POLITICAL ENVIRONMENT

Since the inception of the space age in 1958, when APL first became involved in spacecraft development through the Navy Navigation Satellite Program, new technology development has been the primary focus of the world's aerospace engineers. It's easy to understand why. Spacecraft are mankind's most sophisticated robots, undergoing stressful vibrations during launch, and then being expected to operate for years in an environment that is not very friendly. Unshielded by the Earth's atmosphere and magnetic field, spacecraft are bombarded by intense ultraviolet radiation that erodes organic materials and by cosmic rays and energetic protons and electrons from the Sun that wreak havoc on silicon-based electronics. The structure is subjected to temperature extremes as large as any environment on Earth. For a low-Earth orbiter, communication with the ground is limited to windows of 15 minutes or so as the spacecraft whips by the ground station a few times a day. And for an interplanetary mission, round-trip communication times needed to simply establish a connection can easily exceed 30 minutes. If anything onboard a spacecraft gets "hosed," we cannot merely sigh and hit control-alt-delete. Reliability and a high level of autonomy are at a premium with even the simplest spacecraft mission.

In the early days of space endeavors (the first decade or so), the pressure of these difficulties to a large extent drove the activities. Everyone understood what President Kennedy meant when he said, "We will do these things not because they are easy, but because they are hard." The government was willing and able to pour money into difficult missions in space, and a high level of failure was understood and accepted. Whole missions were sometimes undertaken just to prove that some proposed technology would work in a space environment. During this period, the methods and engineering

practices, as well as space-qualified materials, mechanisms, and instrumentation were developed to make space ventures doable with a reasonably high degree of success, albeit at great expense by most standards.

These cost pressures led to a second phase in which new technology became less important than the success of the space missions. Since it could be argued that the aerospace industry now knew how to develop workable spacecraft, ever larger missions were conceived to accomplish more and more per spacecraft launch. As the cost of these large and complex spacecraft skyrocketed, the space program became highly politicized and the environment generally shifted to paranoia about a failure. The leadership for space missions at the time became deeply instilled with the culture of risk avoidance as opposed to risk mitigation; i.e., "Don't try anything new on my program. I have a schedule to meet." The level to which this environment extended began to trouble many aerospace leaders, who were concerned that new capabilities were not being developed quickly enough to meet the space challenges they foresaw. They understood that the surface of potential endeavors in space had barely been scratched.

This concern was epitomized in the late 1980s at an AIAA workshop in which the author was an invited participant. The workshop examined possible ways to ameliorate the "advanced technology bottleneck" that pervaded the U.S. space program. One strong recommendation was to move toward a series of small missions to accomplish the same goals that were being attempted by very large, billion dollar missions. In a series of five $200 million missions, we could afford to have one (or even two) fail and still achieve a good measure of success. With this much allowable risk, there would be elbowroom for trying many new advances.

As might be expected, the government didn't instantly jump to implement the workshop's suggestion. Nevertheless, the ensuing series of events in the early 1990s rapidly drove them to the point where they simply could no longer afford the big missions. With current federal budgets, NASA and DoD are struggling to keep their space programs alive. In recent years, government leaders pronounced that to meet the crisis of budget shrinkage they would undertake smaller missions and would rely on new and innovative technology to accomplish what once was done through large government expenditures. Voila! A destination reached by any road is the same destination.

We are now in the early stage of an era in which advances in space technology are exceedingly important to our ability to further investigate and understand space and apply that knowledge to societal needs. Performing difficult missions like the exploration of Mercury and Pluto with the limited public moneys now available for such ventures requires very high-tech solutions and a good deal of innovation in the engineering process.

At the same time, "standard" space technology has matured to the point where commercial investment in space-based assets is now practical. Even a midsized company can raise the $40 million or so needed to successfully build and launch a small spacecraft, and large corporations are actively investing on the order of $1 billion to put up large constellations. Commercial space investment applying standard technology (developed and paid for by the government during the previous 30 years) is now larger than government spending in unmanned space and is projected to swamp government spending in the future.[1,2] The current environment thus presents an interesting dichotomy in terms of opportunities: The application of tried and true, yet relatively high-tech methods is leading to enormous commercial spacecraft activity, while difficult missions (e.g., the exploration of other bodies in the solar system) are still quite risky and require new approaches to keep costs low.

Throughout these various eras, APL has been in the thick of things, credited with an impressive number of new ideas and approaches that were engineering "firsts" in space[3] (see the boxed insert). During the middle, more conservative era, APL was more successful than most in pushing new space methods into practice, concentrating on small, one-of-a-kind, difficult missions requested by our sponsors that nearly always required innovation to keep costs low and schedules short. This experience is precisely what is now needed in the government's space ventures, and the Space Department has been aggressively pursuing new spacecraft technology that will enable seemingly unaffordable new space missions, either by reducing costs or by allowing what is currently not technically feasible.

APL'S ADVANCED TECHNOLOGY PROGRAM PHILOSPHY

For efficiency of approach, the Laboratory has adhered to a few fundamental unifying themes in its advanced space technology efforts that serve to glue its projects together and provide a necessary framework. These themes characterize the Space Department's Advanced Technology Development (ATD) Program for spacecraft, and distinguish it from efforts in other organizations. Each theme will be discussed with a description of some of the supporting work at APL over the past few years. To stay within reasonable bounds, I have limited the discussion to the work associated with advanced spacecraft development. There are other components to our ATD effort such as advanced space instruments and space system applications that are not included here.

APL SPACE FIRSTS

Launch Date	Innovation	Spacecraft
25 Aug 1997	First 24-h/day real-time space weather, from L1	ACE
24 Apr 1996	First hyperspectral sensor in space Closed-loop spacecraft pointing at targets First real-time tracking of satellites from space	MSX
17 Feb 1996	First hemispherical resonant gyro in space First solar-powered spacecraft beyond Mars orbit Most distant man-made object seen from Earth	NEAR
5 Sep 1986	First space intercept of an accelerating target	Delta-180
12 Mar 1985	Bifilar helix antenna	Geosat-A
May 1994	First issuance of Announcement of Opportunity electronically (Internet)	NEAR
16 Jul 1982	Autonomous satellite navigation by tracking GPS (GPSPAC R/PA)	Landsat-D
30 Oct 1979	First attitude and command systems using microprocessors "Aerotrim" boom to counter aerotorques in low-Earth orbit	Magsat
27 Jun 1978	Quadrifilar helix antenna with beam shape to compensate for slant range Synthetic aperture radar downlink	Seasat
27 Jun 1978	First microprocessor system in space	Seasat Altimeter
27 Jun 1977	Satellite-to-satellite tracking by Doppler signals (NAVPAC)	1977 56A
12 Oct 1975	Crystal oscillator with all drift removed by programmable synthesizer First use of pulsed plasma microthrusters in space Worldwide time synchronization to 40 ns from a single satellite	TIP-II
7 May 1975	Delayed command system	SAS-C
9 Apr 1975	First satellite-to-satellite tracking	GEOS-C
2 Sep 1972	First satellite compensated for drag and radiation pressure Single-frequency refraction-free satellite navigation Quadrifilar helix antenna	Triad
12 Dec 1970	Dual-spin control of satellite pointing	SAS-A
11 Jan 1968	Heat pipes for spacecraft thermal design	GEOS-B
1 Jul 1967	First yaw stabilization of a satellite using pitch axis wheel	DODGE
29 Nov 1965	Magnetic spin/despin system	DME-A
6 Nov 1965	First integrated circuits in space First heat pipes in spacecraft	GEOS-A
16 Jun 1963	Gravity gradient stabilization Automatic temperature control of spacecraft	Transit 5A-3
19 Dec 1962	First uplink authentication system	Transit 5A-1
31 Oct 1962	Sublimation switches First gallium arsenide solar cell experiment	ANNA-1B
15 Nov 1961	Damping of satellite libration by lossy spring-and-mass	TRAAC
15 Nov 1961	Spacecraft spin imparted by solar pressure vanes	Transit 4-B
29 Jun 1961	First nuclear power supply in a spacecraft First triple-satellite launch	Transit 4-A
21 Feb 1961	First satellite electronic memory	Transit 3-B
22 Jun 1960	First dual-payload launch	Transit 2-A
13 Apr 1960	Two-frequency method for correcting ionospheric error First attitude-controlled spacecraft using permanent magnets Solar attitude detectors Hysteresis damping of satellite libration	Transit 1-B
17 Sep 1959	Yo-yo despin mechanism	Transit 1-A
(1958)	Development of satellite Doppler Navigation System	—
4 Oct 1957	Satellite tracking by Doppler	Sputnik-1

ACE = Advanced Composition Explorer; MSX = Midcourse Space Experiment; NEAR = Near Earth Asteroid Rendezvous; GPCPAC R/PA = Global Positioning System Package Receiver/Processor Assembly; NAVPAC = Navigational Package; TIP = Transit Improvement Program; SAS = Small Astronomy Satellite; GEOS = Geodetic Earth Orbiting Satellite; DODGE = DoD Gravity Gradient Experiment; ANNA = Army, Navy, NASA, Air Force; TRAAC = Transit Research and Attitude Control.

The author adds the following caveat: The fundamental approaches described in this article are not unique. Other organizations have worked on different approaches, and within APL—as might be expected in a high-caliber technical organization—there are differing opinions on how future spacecraft development can best be improved. Nevertheless, after intense internal review and discussion, the approaches highlighted in the following sections have emerged as our framework. As the Program Manager for all of the Space Department's ATD programs, I can truly say that once our direction was set, everyone pulled together to support the effort in a manner that belies any controversy. Many people in both the Technical Services Department (TSD) and Space Department have contributed to the work, and a more detailed acknowledgment is included at the end of the article.

Scalable Architecture

One key to major cost savings is the level of reuse that can be achieved in spacecraft design. A seductive solution to cost reduction is the concept of a universal spacecraft bus, a standard spacecraft shell whose design is frozen and can be used continually by having instruments or other mission-specific packages attached for the ride. This approach has never really worked very well because each bus resource, such as power or data storage, must be overdesigned to handle all possible missions. This eliminates the possibility of systems-level trade-offs of the precious onboard resources to achieve mission goals with a minimal launch weight, the easiest operational demands, the highest reliability, or whatever other parametric constraints dominate the mission requirements. In the past few years NASA has tried to overcome this limitation by cataloging a number of existing spacecraft for rapid acquisition if an existing design happens to match the requirements for a particular misssion. A number of aerospace companies are submitting proposals to be included in this catalog. A mission match in the catalog can lead to considerable cost savings for that mission.

I believe the correct approach to high reuse is to design the fundamental spacecraft architecture to be inherently scalable. That is, develop an architecture such that increasing or decreasing the capacity of all spacecraft resources can be done with minimal changes to the fundamental building blocks (or primitives) of the spacecraft. Thus, for example, we would increase redundancy and the resulting overall reliability by adding more copies of the critical primitives in such a way that there is essentially no impact on the spacecraft block diagram. The primitives themselves must be designed to be standardized building blocks that can be used with minimal design change over a wide range of missions.

The past and current industry methodology for spacecraft implementation is to integrate subsystem packages (boxes) into a spacecraft structure and then interconnect them with harnessing. Power switching is generally centralized, with power carried through the harnessing to individual boxes. Although making things smaller and cheaper within this architecture helps, the approach is inherently weight- and complexity-limited by harnessing, boxes, connectors, mounting structures, and "spaghetti" communication paths. Whole boxes must be removed if rework is required after integration. More importantly, changing requirements from mission to mission necessitates continual redesign of subsystems, boxes, structure, and harnessing because the architectures are inherently not scalable.

After 40 years in the business of developing spacecraft, new technology and new methods entailing risk are still the lifeblood of the Laboratory's contributions to the national space program.

The concept we are working toward (loosely referred to in the Space Department as the IEM or Integrated Electronics Module) is intended to promote high reuse in the next generation of APL spacecraft.[4] Its central idea is to eliminate the subsystem concept and utilize a set of standard-sized boards as new spacecraft primitives for all the core electronics (including RF functions). These boards are integrated by plugging them into one or two card cages, communicating and being powered over a redundant, fault-tolerant backplane. The backplane/motherboard host would accommodate one or more identical processor cards, and allow communication among all spacecraft elements over a redundant high-speed serial bus using memory-mapped addressing. Instruments spread over the spacecraft would be connected to the backplane through standard interface cards that plug into the card cage. This approach lends itself to a distributed, loosely coupled multiprocessor system, which is a scalable and, I believe, preferable means to achieving a high processing capability onboard the spacecraft. Embedded microprocessors can be easily used wherever appropriate in the instruments or on the cards. Receiver and transmitter cards that are adaptable to a range of communication bands without major redesign are housed in the same card cage. We envision the card cage as eventually being part of the structure itself, rather than a box that mounts on a bulkhead.

One can achieve changes in computing power, redundancy, science payload, data storage, communication bands, and fault tolerance by increasing or reducing the number of cards in the IEM without any significant change to the block diagram. Furthermore, as electronics integration, packaging, and connector technology methods improve, the benefit can be realized by simply building the same primitives as smaller cards within the same architecture. However, a number of engineering issues are associated with such an approach, some of the more important being as follows:

- Heat must be removed from the card cage, and localized hot spots due to high power dissipation (on the processor cards especially) must be dealt with.
- Electromagnetic interference between cards, especially between the RF and processor cards, must be considered.
- Testing must be done at the card level versus the card-cage level. The old subsystems were defined in a way that made stand-alone functional and environmental testing of the boxes before delivery to the spacecraft a natural approach. Dealing with card-level primitives that must be plugged into a motherboard to function with other cards requires new approaches to integration and test flow scheduling. Some of the testing challenges are offset, since a failed board can be replaced more easily very late in the program schedule by swapping a spare into its motherboard slot.
- Carrying unregulated power on the backplane raises issues at the spacecraft level in power conversion, isolation, grounding, and noise coupling.
- The high-speed serial communication bus implemented on the backplane must have a standardized interface and be truly fault tolerant. To accomplish these goals we chose the IEEE 1394 standard and elected to implement the interface as a custom VLSI chip that supports a redundant bus, with no requirement for switching sides if one bus fails. This proved to be a challenging development, albeit a powerful feature of the architecture.

These issues have been worked over the past several years, and a demonstration card cage and motherboard with two real and several dummy cards has been developed and flight qualified to resolve the associated engineering problems. The first version, shown in Fig. 1a, was built by TSD using lightweight composite material containing thermally directive fibers to control heat dissipation. The remaining ongoing effort now mostly involves the implementation of the fault-tolerant 1394 communications bus, which will be described later. A second version of the IEM architecture,[5,6] shown in Fig. 1b, is being implemented using miniaturization techniques that have been developed with TSD as another component of our ATD Program, leading us to the following discussion.

Chip-on-Board Packaging

Size and weight are premier factors in spacecraft design. Launch costs per pound are so high that weight considerations dominate spacecraft development. Several years ago the Space Department targeted the size and weight of our flight electronics for an improvement of at least 1 order of magnitude, and preferably 2. At that time our packaging methods were the chief limitation to reducing electronics weight, and in a partnership with TSD, we decided to aim at chip-on-board (COB) as a future method of fabricating our space electronics. For those not familiar with this term, COB means eliminating packaged parts and mounting bare silicon dice directly on printed circuit boards. A recent issue of the *Technical Digest* (Vol. 20, No. 1), devoted entirely to advanced packaging work at APL, provides many excellent articles about this technology and the recent effort in COB (see also Refs. 7–12). Therefore, minimal technical detail is covered here, but the effort is broadly critiqued to put it into the context of our overall program.

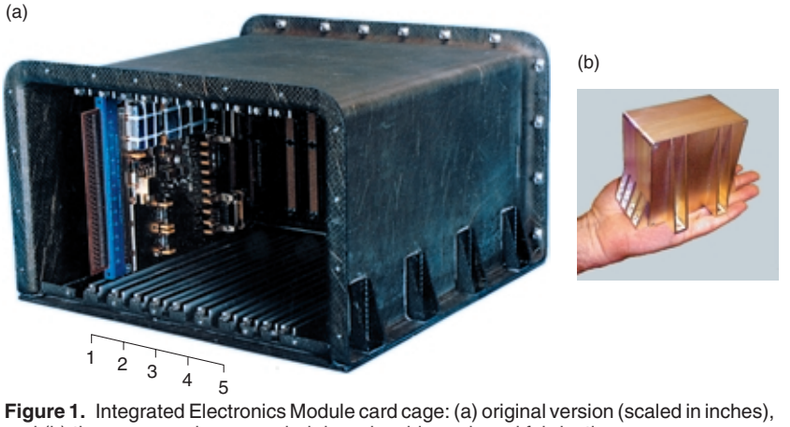

Figure 1. Integrated Electronics Module card cage: (a) original version (scaled in inches), and (b) the same card cage scaled down by chip-on-board fabrication.

There were three main reasons we decided to focus on the COB approach and made a significant investment toward the goal of a flight-qualified COB manufacturing process. First, the approach did not overlap other NASA packaging ATD efforts. When the effort began, the major focus of the NASA centers was on various types of multichip modules (MCMs), which are hermetically sealed packages a few inches on a

side that contain several bare dice assembled on a substrate. MCMs are then mounted on circuit boards like large packaged parts. Second, COB represented a revolutionary rather than evolutionary step in our packaging goals. This is a general characteristic we strongly desire in our internal ATD Program, but the environment in which we find ourselves, as described earlier, inevitably throws roadblocks into plans too lofty. It was hard to resist a chance to aim at a bold change that produced the highest weight/volume payoff of the available approaches. Furthermore, we knew that much improvement in our fabrication capability would spin out of such an effort, even if the ultimate goals were not reached. Finally, and most importantly, COB provides maximum flexibility in the use of components. Some parts in bare die form are very expensive, if not downright impossible to acquire. Properly implemented, the COB process allows small-outline packaged parts, or even MCMs where appropriate, to be mixed on the same board with bare dice so that each part can be optimally selected as packaged or unpackaged.

The entire goal of the COB effort has been to develop a process for fabricating flight-qualified electronics using bare dice on boards. The word "process" means something very precise in spacecraft development: a documented, detailed methodology for manufacturing that is highly repeatable and reliable, independent of "special" key personnel, and transportable to other organizations. The success of the process may require highly skilled personnel, but shouldn't depend on that one indispensable genius to make it work. Such a process has all the same qualities as those touted by software engineers, who for years had pleaded on the deaf ears of their management for a disciplined and rigorous process to produce reliable, maintainable software on schedule. In the case of COB, many technical issues had to be solved for such a flight-qualified process to be in place. An example is the ability to protect the assemblies from contamination, which can cause component corrosion.[8,11]

The Space Department and TSD jointly undertook the development of the COB flight process. We were helped by grants from NASA Goddard that provided crucial financial support to supplement the Laboratory's investment, as well as very important moral support from Goddard technical personnel. The early approach was to rebuild to flight standards an existing APL electronic subsystem that flew on the Freja spacecraft. No changes were made to the electrical design or the parts used other than to acquire as many as possible as bare dice and then rebuild as COB. This was the ultimate in "learn by doing" with many failures along the way. By the time the APL shops had solved most of the problems and successfully built some flight-tested COB assemblies several years later, a real process had been largely defined. The final touches are still being worked into the current version.

The COB payoff in weight and volume has been significant, just about the initial factor of 10 we hoped for. Figure 2 shows the size reduction of a typical multilayer board of packaged parts when it is fabricated as COB. The IEM card cage shown in Fig. 1a is reduced to something like the one shown in Fig. 1b when fabricated by the current COB process. However, this process is just a step along the way to the author's real goal for APL electronics. The first hurdle is to eliminate chip carriers. The next step is to eliminate boards and substrates that constrain us to two-dimensional interconnects. If we can stack the bare electronic dice, one atop another, and connect them somehow along the edges or through the stack, then our electronics become little cubes of silicon.[13] The new IEM spacecraft electronics primitives become the individual chips, and the communication/power distribution backplane becomes something akin to built-in connectors along the edges of the cubes. If we can make such an approach viable for space, then we are really getting somewhere in miniaturization. Such an approach requires at least two other technology advances:

1. The ability to replace an aggregate of commercial parts with a single custom VLSI chip that provides a natural primitive function in the same vein as a current IEM board
2. Ultra-low-power (ULP) versions of these CMOS chips so that the cubes do not overheat

Custom VLSI Electronics

For the past decade or more the Space Department has engaged in developmental projects in custom VLSI, designing application-specific integrated circuits (ASICs)

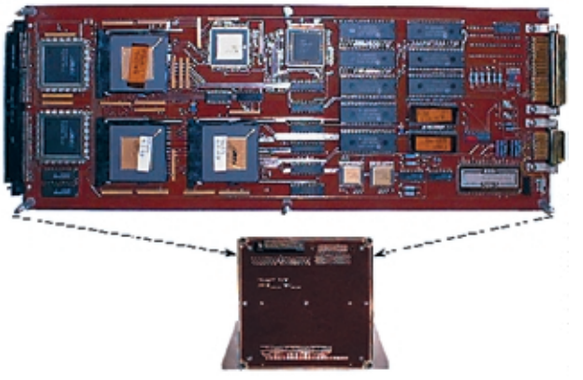

Figure 2. Relative size reduction using COB fabrication shown in Fig. 1b. The two boards hold identical electrical designs, the upper being an electrical breadboard for testing the design built using current APL multilayer board processes.

to be fabricated by commercial silicon foundries. Several of these chips have been used in past spacecraft programs; however, until the 1990s, the radiation susceptibility of foundry-produced chips has impeded their widespread use in spacecraft. Five years ago, a major step forward in CMOS radiation resistance occurred with the emergence of cost-effective commercial foundry sources of radiation-resistant bulk CMOS VLSI devices. Over several subsequent years, in the Space Department's Independent Research and Development Program, we benchmarked the radiation resistance of these new foundry processes. We have also experimented with new VLSI circuit design techniques to improve latch-up resistance and to achieve mixed analog/digital functionality on the same chip.[14–17] In addition, there are now emerging commercial field-programmable gate arrays (FPGAs) which have high radiation tolerance.

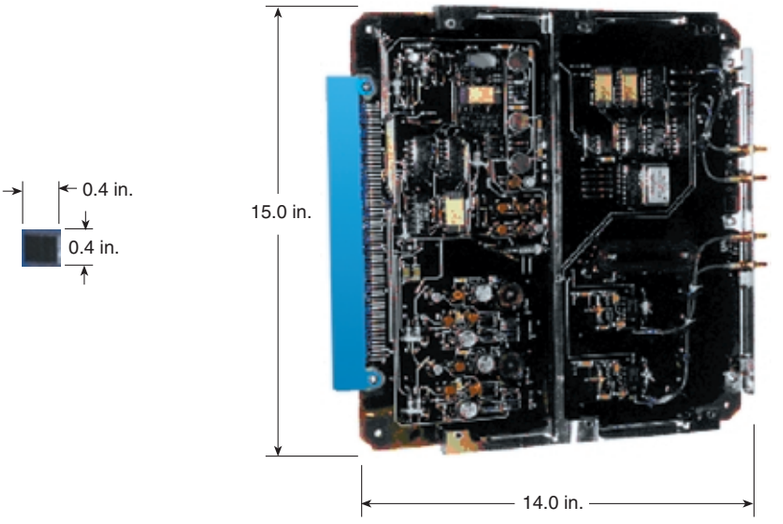

Figure 3. Improvements gained by integrating all required analog/digital electronics into a single, mixed-mode CMOS devise are obvious when comparing the APL time-of-flight (TOF) measurement chip on the left with the standard TOF system on the right, which was used on Cassini, ACE (Advanced Composition Explorer), FUSE (Far Ultraviolet Spectroscopic Explorer), and other spacecraft.

In short, the Laboratory's long and patient effort in moving toward custom-designed ASICs for space is poised for a real explosion if we do the right stuff. The ASIC products now coming out of this part of our ATD Program have what can only be described as a startling impact on our spacecraft electronics. Our latest radiation-resistant time-of-flight (TOF) chip, for example, replaces an entire board of discrete analog and digital components and reduces power by more than an order of magnitude over the traditional approach.[18] (The measurement of the TOF of charged particles is a crucial capability of instruments for mass and particle spectroscopy, ultraviolet imaging, and range finding.)

Figure 3 shows the complete picture of the TOF chip payoff, and can leave little doubt as to why I have carried this vision for over 15 years. Comparing the APL TOF chip (with all analog and digital electronics in one chip) and a standard TOF system (all analog and digital electronics typically on a double-sided board), weight is reduced from 240 to 3 g, resolution is enhanced from 750 to 100 ps, power is reduced from 1000 to 25 mW, and radiation hardness is increased from 100 krad to 1 Mrad. In addition to such huge improvements, the reliability of electronics is actually improved by higher levels of integration. The entire space industry needs to move toward chips as spacecraft primitives instead of boards or, heaven forbid(!), boxes. However, there are remaining hurdles that are nontrivial.

Although the technology for custom analog and digital chips stands poised to completely change the "ballgame" in spacecraft electronics, we are seriously limited by the number of people who can perform such designs and who fully understand this approach. A problem to be overcome (for the entire space industry, not just APL) is the infusion of the appropriate expertise from the relatively small group of people now carrying out these new developments into the engineering staff at large. Many of our experienced and key designers, through no fault of their own, are still locked into the old culture of implementing boards, and we have yet to tap their creative energy in using custom chips as the new spacecraft primitives. This change requires training through hands-on developmental chip projects and easier access to existing VLSI software design tools. The author's vision for the Space Department in the next 5 years is to move almost entirely over to this approach, a difficult undertaking that requires resources and entails risk.

One of those risks concerns the stability of the commercial foundry sources for radiation-resistant custom chips. The space industry is not a mass market by any stretch of the imagination. After investing in a very high-tech process, it's hard for a commercial silicon foundry to make money on customers who want only a half dozen radiation-resistant parts. They would prefer to fabricate 10 million or so parts for cellular phone manufacturers who have no need of radiation resistance. This problem requires the attention of both NASA and DoD. The federal government, mainly through the Defense Advanced Research Projects Agency, helped create the silicon foundry industry in the 1980s, and it is in their extreme interest to keep

radiation-hard foundries in business for the country's space program. This is the scariest problem for APL, mainly because the Laboratory has no control over it.

Another hurdle is similar to the COB problem and is something the Laboratory could help solve. At present, the development of custom chips is more like an R&D activity than an established technical process. It is more expensive to develop a flight-qualified custom chip than the equivalent electronics as a flight-qualified board. A well-defined and repeatable flight-qualified process is lacking for custom chip development, whether it involves a radiation-hard FPGA or a pure custom analog VLSI chip. Part of such a process involves the establishment of software tools that sufficiently automate the design process. Such commercially available tools are emerging, but they are very expensive and invariably have limitations that frustrate designers and cause hang-ups. The lack of a predictable chip development process introduces both cost and schedule risks to spacecraft programs.

Despite these obstacles, I am confident that the culture of spacecraft design engineers in the near future will be to think in terms of developing a spacecraft electronic function as a VLSI chip, rather than as a board or a package. With the three-dimensional stacking possibilities offered by the advanced packaging methods now being perfected, we can truly envision a future complex electronic system on a spacecraft as a tiny cube.

Advanced Power Systems

The Space Department has just begun a technology effort involving advanced power systems, which I expect will grow significantly in the next few years. It is driven by a push toward ULP CMOS electronics throughout industry and academia. Since it is essentially out of the question politically to fly small, nuclear power sources on spacecraft, we are relegated to carrying heavy, low-efficiency solar arrays and batteries. This puts us all in the position of being chronically power starved in designing a spacecraft, and everyone (especially the spacecraft system engineer) is delighted at anything that can reduce power demands onboard. However, in my view, the impact of ULP, and the real opportunity for payoff, does not lie in simply scaling back the size of the spacecraft power system. Rather, ULP electronics offer the opportunity to completely change the architecture of spacecraft power systems. Some background is helpful to an appreciation of this argument.

The power dissipation of electronics is proportional to the square of the supply voltage, typically 5 V for today's CMOS. The thrust of ULP research is to drive the required supply voltage down to values as low as 0.1 V. Let's assume this effort will eventually succeed, and that essentially all the internal electronics will take zero power. We still will not have a major effect on spacecraft power system weight, simply because other power needs dominate the onboard requirements. These needs come from communications to the ground, momentum wheels to control attitude, firing thrusters, and the like. What, then, is the big advantage of ULP? It opens the possibility of going to a distributed onboard power system rather than the central system traditionally flown.

The traditional system (typically) operates everything onboard off a 28-V bus supplied by solar cell arrays in which cells are wired in series to produce the needed voltage level. The battery cells are likewise so designed. Voltage-regulation electronics is required to maintain the bus within acceptable limits. Redundant subsystems (or boards in the IEM approach) are powered on and off through banks of switches connecting them to the power bus, and the 28-V power is DC-DC converted down to the specific levels around the 5 V needed by each electronic subsystem. The power converters are generally inefficient and heavy, the switching must be designed to avoid failure in the "on" condition, and, to prevent an electrical short from killing the whole system, fusing is required in all circuits.

The same techniques now being explored to allow extremely low electronics supply voltages may be directed to achieving a more modest decrease (say to around 1 V), accompanied by a proportionally much wider tolerance to supply voltage variations. This would open the possibility of using battery-driven electronics, where the individual electronics primitives in the spacecraft could each survive 5 or more years (like your watch) off a small primary cell. (Primary, nonrechargeable cells have generally much higher energy density than their secondary, rechargeable counterparts.) In such an approach, many switches and power converters would be eliminated. A failure in a redundant piece of electronics would not require switching or fusing to protect a central power supply, potentially making operation much simpler and easier. Maybe other systems (e.g., a momentum wheel) that would still require solar arrays and a battery could each operate off their own power circuit that was optimally tuned to their voltage requirements, eliminating yet more switches and converters. If the electronic supply voltages are low enough, it might even be possible to tap spacecraft temperature gradients using tiny Sterling engines to produce the needed power (reader, please stop laughing).

Other interesting ideas flow out of this line of thought, but I will stop here since you get the idea. In brief, perhaps a power system comprising many individual, unconnected power circuits, each tuned to its own load requirements, would end up simpler, lighter, and cheaper; it may also be scalable in a more graceful way.

I have no idea if this is true, but wouldn't it be exciting to find out? Along the way I'm sure some great improvements would emerge, like those resulting from our previously described packaging efforts. My instincts tell me that this would be a good approach if the technology could support it. Long ago I became convinced that distributed control invariably works better than centralized control, and I can see an analogy for power.

The Biological Paradigm for Autonomy

As described earlier, a high level of autonomy is important to successful spacecraft missions. However, autonomy must be built on reliability and fault tolerance. In the author's opinion, the correct architecture for building autonomy is to be found in biological systems. Consider, for example, placing your hand on a red-hot stove. You will jerk that hand back before you are even consciously aware of pain, faster than any signal could possibly propagate along relatively slow neurons to your brain. The processing for this reaction is embedded locally in the tactile system, and the same kind of reaction processing causes us to blink if something comes flying at our face. Although the brain does a lot of very sophisticated processing to produce high levels of autonomy, a huge amount of sensory information processing occurs right in the eyeball, the optic nerve, and the cochlea of the inner ear, completely independent of the brain. Biological systems thus have two main characteristics that are models for an autonomous spacecraft:

1. Processing is distributed and loosely coupled, and actions are not all controlled by a single giant processor.
2. The sophisticated, autonomous functions performed by the central processor are overridden by simple, hard-wired "safing" behavior that allows the program in the central processor to fail gracefully (i.e., do something stupid like try to touch a hot stove).

The promise of radiation-resistant spacecraft processors with huge processing rates has been around for years, but it will never materialize because the expense of building such electronics is high and the spacecraft market is too small. Consequently, the capability of flight-qualified processors always lags a decade or more behind the processing power of commercial computers. One way to get higher effective processing rates onboard with currently available flight processors is to embed more loosely coupled processors into the architecture. This makes the processing power onboard scalable, which is the goal of our IEM approach. We are now using the Mongoose V flight processor as the IEM processor primitive. If we are doing anything right, switching to a different processor card in the future will have minimal impact on the architecture or the other IEM primitives.

The second characteristic of the biological paradigm is more crucial, and it has been the fundamental approach of APL for years. The message it delivers is that the sophisticated functions implemented in software must be built on a layer of "bulletproof" and highly reliable hardware to provide safing. At the lowest level, this hardware must be simple, finite-state logic so it can be tested for all conditions, and it must be fully redundant in a manner that is fault tolerant. That is, it cannot require ground intervention to keep running through a failure of one copy. This layer of logic provides bare survival in one piece if anything goes wrong onboard.

A second, more sophisticated layer can operate on top of the first, whose job it is to "watchdog" the layer above it, and so on. The most likely component to fail on a spacecraft is the most sophisticated autonomy software, simply because it is the most complex and the hardest to test. Many people claim (frequently for political purposes) that complex software can never be fully debugged. The APL layered approach to autonomy in a sense is designing the system so that the most complex functions can safely fail, even though we work hard to make them reliable. This approach is ingrained in the IEM architecture. We are attempting to design the architecture by assuming that at some point in the spacecraft's life the onboard software will inevitably have a glitch (I'm trying to put this kindly for the sake of our software engineers).

The lowest levels of this layered architecture are, in my opinion, the most difficult, the most critical, and also the most interesting. I believe that if we get the lowest levels working well, almost anything done at the highest, complex software levels will work, with occasional loss of data as the spacecraft "recovers itself." Unfortunately, the highest-level "stuff" is the most enticing to software engineers; at this level, glamorous terms like artificial intelligence and expert systems begin to be bandied about. Yet I am firmly convinced that software experts are the most qualified to define the lowest levels of safing, but this does not always happen. Notice the words "recovers itself" in the statement above. This is the next major step that APL should take in spacecraft autonomy. With the correct type of layered autonomy, after a glitch the spacecraft can reliably get going on its own. Up to now the low-level safing in our spacecraft only parks them in a safe power mode and then relies on commands from the ground to get back in business.

Recent APL spacecraft such as NEAR (the Near Earth Asteroid Rendezvous) and MSX (the Midcourse Space Experiment) have exhibited highly successful safing of this type through the application of rule-based processing at the lowest levels (decisions based on multiple-clause rules applied to telemetry data[19]). Autonomy experts are now suggesting that model-

based reasoning (i.e., decisions based on a comparison of observed spacecraft behavior to an onboard digital model of the spacecraft) is superior. For this new area of investigation, the Space Department is joining forces with the APL Research and Technology Development Center to focus on spacecraft modeling. However, the use of model-based reasoning at the lowest levels of the layered autonomy architecture conflicts with the stringent requirements of simplicity, reliability, and fault tolerance. The lowest levels of spacecraft safing cannot be eliminated or migrate to model-based processing. This type of processing must be relegated to the highest software level for complex decisions that generally do not involve survival.

Within the IEM, the first low-level element that must be fault tolerant is the 1394 serial communication bus. We began development of a single-chip interface to a redundant backplane bus (two channels) whereby if either channel failed, the interface would continue to operate on the other channel with no ground intervention. There are two versions of the IEEE 1394 bus standard—cable and backplane. We specifically selected the simpler backplane version because the issues of fault tolerance and "node clobbering" (i.e., one node clobbering the software on another node) were more complex in the cable version. The development of this ASIC, which APL calls the bus interface unit chip, has gone through several design iterations and is nearing final form. Handling all possible cases to make it truly "bulletproof" has been difficult. The IEM architecture includes a special card primitive called the safer card, which will have access to all 1394 bus transactions and to the command processing on the receiver card. In addition, it will implement the low-level rule-based safing functions mentioned earlier. This is a currently active area of IEM development.

FINAL REMARKS

Alas, we must stop here for the editor's axe, having discussed only a portion of the Space Department's efforts in ATD. Other DoD-oriented ATD activities are going on that I have not touched upon. Embryonic efforts are under way that involve much more interesting and speculative ideas. One of these is for a spacecraft that would live for 100 years. This is the sort of lifetime needed to reach the nearest star or to stand as a sentinel that could give early warning of dangerous near-Earth objects. My approach to such a requirement would be to again fall back on the biological paradigm—the spacecraft, like our bodies, would repair itself. Some techniques to achieve this goal might be to periodically raise the temperature of the electronics to anneal radiation damage, or to make all the electronics microprogrammable so that failures could be eliminated by self-reconfiguration. This one requirement to make a spacecraft live longer than a person is interesting enough to be the subject of an entire future article.

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The jury is still out on most of the material described in this article. The first Laboratory spacecraft using the card-cage approach for the core electronics is TIMED (Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics), which is scheduled for launch in early 2000. Doing things this new way did lead to test and integration difficulties as expected. In the past 24 months, the IEM approach was proposed for three very different missions for the NASA Discovery Program in interplanetary science. We found that the architecture was indeed applicable to all three missions with very little difference, leading us to believe we are on the right track toward a truly scalable approach.

The general environment for using advanced technology and new methods in space missions is probably the best it has been in decades. However, an advanced technology "funding gap" still exists that seems politically unavoidable. Under government rules, plans can be developed only so far under R&D-type funding grants, and programs that pick up immature technology still experience a certain level of pain, cost, and risk. There is little doubt that the Laboratory has felt these effects on the TIMED Program's use of the card cage and new card-level primitives for the RF communications system. On the other hand, this is probably as it should be, lest the people working on advanced technology become too complacent. The extreme cost-competitiveness of, for example, the NASA unmanned program definitely discourages new approaches. However, the missions that APL is proposing and will continue to propose cannot be achieved easily without such new approaches. Consequently, we will continue to live in this exciting, yet taxing environment, and justifiably so if we expect to do truly challenging work for our sponsors.

Finally, I would like to acknowledge the many people who performed the work described here, and mention the key people by name. Martin Fraeman has been leading the development of the scalable architecture with a lot of help from Richard Conde. Robert Bokulic has led the effort to develop a new set of card-level primitives for the RF communications functions in the IEM approach. Binh Le has been leading our thrust in

advanced packaging, and Jay Dettmer and his group in TSD have been key to creating a flight-qualified COB process. Kim Strohbehn and Nikolaos Paschalidis have been heading the Space Department's effort in mixed-mode ASICs for some time. The TOF chip described (Fig. 3) was developed by Dr. Paschalidis in collaboration with students from the University of Thrace, Greece. Many of the Space Department's ideas about low-level safing, and surely a good deal of influence on my views, come from James Perschy and Ark Lew, and from Susan Lee, who has since transferred to another department at APL. Ms. Lee has had a valuable influence on the design of the APL dual-bus 1394 bus interface unit chip and on the development of the Space Department's general approach to safing. Ralph McNutt and Robert Gold have recently been developing mission concepts for spacecraft visiting a star or acting as sentinels against dangerous near-Earth objects.

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