The Case for Plastic-Encapsulated Microcircuits in Spaceflight Applications

Andrew F. Moor, Anthony Casasnovas, and Stanley R. Purwin

The Applied Physics Laboratory has successfully selected, handled, screened, qualified, and reliably applied plastic-encapsulated microcircuits on multiple artificial satellite applications. The approach outlined in this article describes in detail the risks associated with using these commercial devices in spaceflight applications and the techniques used by APL to mitigate against potential causes for concern. The Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics (TIMED) Program is used to describe the APL approach.
(Keywords: Commercial off-the-shelf (COTS), Handling, Plastic-encapsulated microcircuit (PEM), Qualification, Screening.)

INTRODUCTION

At APL, we most commonly associate the term plastic-encapsulated microcircuit (PEM) with commercial off-the-shelf (COTS) devices, except that a PEM has a plastic package. Please note that a handful of PEMs can be found on the Qualified Manufacturers Listing (QML) and therefore cannot be classified as COTS. For the purpose of this article, PEMs can be microcircuits, semiconductors, passive components, or otherwise. COTS devices, in turn, are any commercially processed components. Historically, PEMs were never considered to be suitable for spaceflight applications because of their commercial connotation. However, with the decreased availability of military-grade hermetically sealed components, PEMs have become a necessity.

APL's decision to use PEMs is founded on both internal and external factors. Internally, there was the need for state-of-the-art technology. For example, PEMs were the enabling technology for the development of the Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics (TIMED) Program's 2-GB solid-state recorder. Only by using commercially available high-density memory devices could the size, weight, and cost constraints of the TIMED mission have been achieved. The internal need for such technology was motivated by external customer demands for a "faster, better, cheaper, and more reliable product." As a result of these factors, overall product life cycles have been reduced, leading to the decrease in availability and rapid obsolescence of once desirable military-grade devices.

Although suitable PEMs were found for TIMED, they may not be available for every high-reliability application. The risks associated with using commercial

technology must always be balanced against the need for space-level component reliability. PEM use is expected to continue to increase over time as the risks associated with these devices are fully understood.

The TIMED Program is the first mission in NASA's Solar Connections Program. TIMED will explore the Earth's mesosphere and lower thermosphere in the 60- to 80-km range. It has a 3-year development cycle, followed by a 2-year mission life; launch is expected in January 2000. Key technical accomplishments for TIMED besides the 2-GB solid-state recorder noted previously are a radiation-hardened 32-bit RISC processor; redundant MIL-STD-1553 data bus; and the integrated command, telemetry, radio-frequency communications Global Positioning System and data storage module.

More specifically, Table 1 provides a breakdown of the electrical, electronic, and electromechanical parts that comprise the TIMED spacecraft. The numbers are representative of unique line items; multiple occurrences of a device are not shown. The military parts referred to in Table 1 include those that meet all MIL-STD-883, QML (including QML PEMs), Defense Electronics Supply Center-Standard Military Drawing, and NASA specifications. Source control drawings include internal purchase drawings, parts tested to a purchase order requirement, and parts tested to a manufacturer's high-reliability flow. The COTS devices, which include PEMs, represent 16% of the total line items used on the TIMED Program.

PEM SELECTION CRITERIA

The Laboratory uses a four-step approach to part selection: concurrent engineering; evaluation of each part for its intended application; partnership with world-class suppliers; and review of the manufacturer's reliability data. An effective parts management program begins with a concurrent engineering effort. Key team players must represent the following disciplines: design, manufacturing, component reliability, logistics, and purchasing. The team is responsible for evaluation of each part selected for its intended application. Note that a PEM that is suitable and qualified for a particular application on a spacecraft may be completely unusable in another application on the same spacecraft! This simple concept is often overlooked by design or components engineers who are accustomed to approving parts solely on the basis of military designation and not their intended application.

To help simplify the selection process, efforts are made to form partnerships with only a select handful of world-class suppliers. The rationale behind limiting vendor selection is based on several reasons:

- It ultimately reduces the number of parts that must be evaluated by the engineering team.
- It facilitates the working relationship between APL and the manufacturer.
- It allows APL to maintain good and reliable contacts that are crucial to overcoming the service aspects of being identified as a small-volume customer.

Regarding the last item, APL needs access to manufacturers' reliability reports and technical staff. The TIMED Program has very specific requirements regarding vendor selection and PEM reliability. As such, the adequacy of a given manufacturer's reliability report ultimately becomes the basis for acceptance, as well as the foundation for the screening and qualification regime employed by APL.

Table 1. TIMED parts breakdown.

Parts	Military	SCD	PEM	COTS
Capacitor	124	1		3
Connector	38	31		47
Diode	27	1		3
Magnetics	8			11
Microcircuit	134	11	8	4
Oscillator	4	4		4
Relay	2	6		
Resistor	321	21	7	24
RF devices	4	19		24
Transistor	12	4	1	3
Miscellaneous	34	21		15
Totals	708	119	16	138

Note: SCD = source control drawing, PEM = plastic-encapsulated microcircuit, COTS = commercial off-the-shelf.

PEM HANDLING ISSUES

As with PEM selection, APL employs a four-step approach to handling: use of finger cots and gloves; moisture protection; conformal coating; and adherence to electrostatic discharge (ESD) sensitivity practices and procedures. The rationale for taking such precautions is corrosion avoidance.

For galvanic corrosion to occur in PEMs, the following elements are necessary: a bimetallic couple, most often gold/aluminum, present in the gold bondwire to the aluminum metallization pad; free mobile ionic contamination, usually chlorine, potassium, bromine, and/or sodium; and moisture, diffused from the atmosphere, to form an electrolyte.[1] Except for the newly released copper/copper circuit designs, which we have not studied here (and may not be available as a PEM), the bimetallic couple is present in all PEMs. We therefore focus our efforts on reducing ionic contaminants and moisture.

We can identify two sources of ionic contamination. Traditionally, the encapsulant material was the main source of ionic contamination within the PEM. However, today's molding compounds are considered ion-free, since the typical ionic residue level of such parts is less than 10 parts per million.[2] The second potential problem is incidental contamination, which is external to the PEM. This contamination can come from the atmosphere, human handling, cleaning agents, etc.

The ionic transport of incidental ionic contamination to the die surface is still the subject of intense debate. The addition of up to 80% silicon fillers to produce the epoxy/novolac encapsulant used today in most PEMs limits ionic mobility. The encapsulant material manufacturers reacted to this limited mobility by adding an "ion getter" or scavenger. The incorporation of alkali- and halide-ion gettering agents into the epoxy molding compound prevents migrating ions in the epoxy from contaminating any diffused or accumulated water in the package.[3] The diffusion of ionic contaminants through an epoxy/novolac encapsulant is discussed in the following section.

The Case for Finger Cots and Gloves

The case for finger cots and gloves is strong. Figure 1 shows data from a recent University of Maryland Computer-Aided Life-Cycle Engineering (CALCE) Electronic Packaging Research Center study.[4] The study has demonstrated that the rate of ionic diffusion through the encapsulant is a function of the ionic concentration, the epoxy/novolac formulation, and the additives in the epoxy/novolac. This study was conducted by separating two cavities with a slice of epoxy/novolac; CALCE personnel filled one cavity with distilled water and the other with a solution of ionic contaminants. They evaluated various combinations of ionic species, concentrations, temperatures, and epoxy formulations. The diffusion rate of ionic species throughout the encapsulant was measured by sampling the distilled water and analyzing it.

Two points can be gleaned from Fig. 1. First, since the diffusion rate is directly related to ion concentration, it becomes necessary to limit the introduction of any external contaminants, thus justifying the use of finger cots or gloves. Second, the use of ion getters impedes the diffusion of ions. Unfortunately, it can be seen that such ion getters are a limited resource and must be preserved. As shown in Fig. 1 for the two highest NaCl concentrations, after approximately 18 days, the ion getters were completely exhausted and the solutions reached equilibrium.

What is cause for concern about the University of Maryland study[4] is that it was based on epoxy/novolac slices of approximately 30 mils. How much time does a device (e.g., the one shown in Fig. 2) have before ionic contamination occurs if only approximately 6 mils of separation exist between the PEM surface and the bondwires? Hours may pass, not days, before ionic contamination could travel along the bondwire to the surface of the die under similar conditions. The authors anticipate a much slower ionic diffusion rate for PEMs under normal use because the moisture available will be limited and far less than in the CALCE study.

The Need for Moisture Protection

Moisture protection techniques are required for two distinct reasons: (1) to alleviate any potential "popcorning" of PEMs during the fabrication process (e.g., package cracking during solder reflow caused by high moisture content in the package[3]) and (2) in general, to combat corrosion. APL's approach to controlling moisture involves timely bake-out of components, environmentally controlled storage areas, and the use of dry boxes.

To prevent popcorning, devices undergo a bake-out of 24 h at +125°C at the conclusion of all incoming inspections unless there are solderability or lead finish concerns. Alternative methods such as vacuum bakes at lower temperatures or extended storage (greater than 30 days) in a dry box may be used.[5] Then, all parts are individually sealed in dry-nitrogen–purged bags before placement in flight stores. Once the dry bag is opened, there is only a limited time during

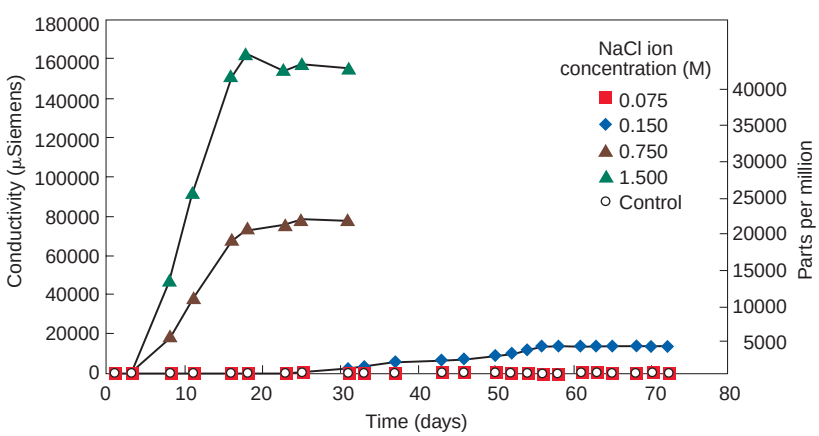

Figure 1. Varying rates of NaCl diffusion through epoxy/novolac as a function of ionic concentration. The test consisted of a 30-mil slice of epoxy/novolac that separated distilled water from a known NaCl solution. Testing was performed at 85°C. The diffusion rate of NaCl through the epoxy/novolac was measured by sampling the distilled water and analyzing it periodically. Note that no diffusion occurs for several days. (Reprinted, with permission, from Ref. 4.)

Figure 2. Samsung 32-MB flash memory. Note the proximity of the bondwire loop to the top surface of the PEM.

which the part can be soldered before it must be baked out again. The actual time allotted (out-of-bag time) varies for each part and is a function of the moisture sensitivity level ascribed to it in accordance with Interconnections Packaging Circuitry Standard IPC-SM-786A.[6]

To combat corrosion, we have already explained how finger cots or gloves can help reduce external contaminants. However, since all sources of ionic contaminants cannot be eliminated, additional preventive techniques must be employed. The focus of these techniques is moisture avoidance.

Recall that moisture serves as the transport vehicle that allows ionic contamination to reach the surface of the die. The simplest methods to minimize moisture ingress have already been discussed (i.e., dry-nitrogen–purged bags and bake-out of PEMs). Reliance solely on a dry bag for protection is insufficient, however. Cleanliness and moisture avoidance are conjoined. An APL study has demonstrated that dry bags serve only as barriers to moisture, not to air.[7] Data from the study show noticeable air exchange occurring within a 1-week period and complete air exchange occurring within 1 month. To ensure cleanliness, parts must be maintained in environmentally controlled storage areas or dry boxes until they are needed. These boxes can be used, as long as it is practical, during piece-part testing, during board fabrication, and before and after conformal coating.[8] In fact, entire printed wiring board (PWB) assemblies can be placed in the dry box.

The Need for Conformal Coating

The Laboratory has performed numerous studies, reviewed industry data, and continues to conduct additional studies in this area. Our results have shown that delamination can be present in devices "as-received" from the manufacturer (see Fig. 3).

Although differing opinions exist regarding the validity and concerns associated with delamination, APL will continue to take a cautious approach until definitive answers can be ascertained. When a PEM exhibits large delaminations, we assume that these are a path for moisture and contaminants to reach the surface of the die by traversing along the lead frame and bondwires; therefore, we need conformal coating to seal this path. Conformal coating is known for increasing the reliability of assemblies containing PEMs.[9] Although conformal coating will not prevent moisture diffusion entirely (only slow it down), we speculate that it will preserve ion getters by filtering out some ionic species. The specific conformal coating recommended by APL is Parylene.

The choice of Parylene is based on a study conducted by the APL Full Signal Translator (FST) Program as well as other industry data.[9] The FST study involved subjecting parts to steady-state temperature-humidity bias life testing (85°C/85% relative humidity or 85/85 testing). Three categories of parts were tested: uncoated PEMs, PEMs with Urelane conformal coating, and PEMs with Parylene conformal coating. After 500-h 85/85 testing, only the Parylene-coated parts were functional.

In addition, a recent chip-on-board (COB) study, also conducted by APL, has validated the recommendation for Parylene. The COB study demonstrated that a Parylene/epoxy combination effectively protected unpassivated Sandia National Laboratories "triple-track" die during 1000-h 85/85 testing.[10]

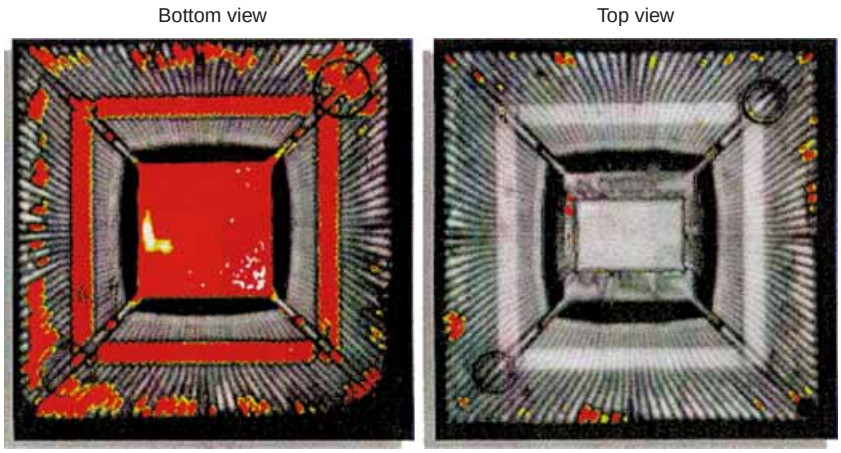

Figure 3. Delamination in the "as-received" condition for an Analog Devices digital signal processing microcomputer; red indicates delamination sites. Notice approximately 100% delamination on the bottom of the lead frame, presenting a possible conduit for moisture to reach the die.

Unfortunately, as with anything beneficial, there are always some drawbacks. Several associated usage issues must be addressed regarding Parylene. For example, Parylene requires a vacuum deposition process. As such, access to appropriate equipment is required. In addition, it is often necessary to mount devices other than PEMs on the same PWB. Some of those devices may not be hermetically sealed or some may be vented. Since effects of the vacuum disposition process on these nonhermetically sealed or vented components are not fully understood, it therefore becomes necessary to mask off certain devices and interconnect pads of the board. Rework also becomes difficult once a device is coated with Parylene. Either mechanical stripping or localized heating can be used to remove a device, but both approaches can cause cosmetic scarring of the PWB assembly. The NASA Goddard Space Flight Center is currently investigating an alternative method for removing Parylene that involves a "fine-nozzle" sandblaster with ionizers to offset ESD concerns.

ESD Practices and Procedures

ESD is an issue independent of PEM use. It is prudent practice to handle all components in such a manner as to avoid ESD damage. APL has an established ESD program that conforms to MIL-STD-1686, "Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment." In addition, local ionizers are recommended to further dissipate electrostatic charges.

PEM SCREENING

For the TIMED Program, individual piece-part testing involves electrical verification (at the mission temperature profile), radiographic examination, and visual and mechanical inspection. All screening tests except for mechanical inspection are performed on a 100% basis.

Electrical Verification

Most PEMs are not rated to meet the standard military temperature range (i.e., −55 to +125°C). This should not be viewed as cause for concern, but a risk to be mitigated. The process that reduces the risk involved in using components or systems outside the manufacturer's temperature specifications has been termed by the University of Maryland CALCE Electronic Packaging Research Center as "uprating."[11]

Most important for the PEM in question is to meet the appropriate mission temperature profile. For TIMED, the most severe environment occurs during spacecraft thermal vacuum testing, −40 to +100°C (actual component temperatures during flight are not expected to exceed +5 to +50°C).

APL does not automatically use a part outside its intended manufacturer's temperature rating in a flight application. In fact, we de-rate components to minimize the occurrence of this possibility. De-rating is defined as a process in which device voltage, current, and power are reduced by a certain percentage to extend longevity. For PEMs, this is accomplished by calculating the maximum power dissipation as a function of the maximum rated temperature. However, if no alternative part is available, one must ensure that the part can function at the temperature profile required.

The choice to uprate comes with various legal consequences. Manufacturers have warned that using a part outside of its intended temperature range will automatically invalidate any implied warranty. Even more serious legal repercussions may exist, including the possibility of lawsuits.

To ensure that a part will function reliably in the intended flight application, APL performs 100% electrical verification at the mission temperature profile extremes. Because little power is dissipated during electrical tests, the device integrity is not compromised. In addition, sample parts are subjected to a selected set of qualification tests. The choice of specific tests is based on a detailed analysis of the manufacturer's reliability data. The purpose of qualification testing is to complement what has already been accomplished by the manufacturer. Ramifications associated with qualification testing will be discussed in more detail later.

Radiographic Examination

Radiographic (X-ray) examination is performed, on a 100% basis, in accordance with MIL-STD-883, Method 2012, "Radiography." APL recommends and uses a real-time X-ray technique to obtain beneficial results. Unlike film, real-time X rays provide high-resolution images in various planes by rotating the devices inside the chamber. This procedure enables the PEM user to develop a three-dimensional abstraction of the device's internal construction. Figure 4 provides an excellent view of the results obtained using the real-time technique. The image is representative of a Samsung 64-MB dynamic random-access memory (DRAM), which is an integral part of the TIMED solid-state recorders. Figure 2 also emphasizes the superior capabilities of the real-time X-ray technique.

The performance of a radiographic examination should not be viewed in the context of pass/fail criteria attributed to lot rejection. Rather, the purpose of performing the examination is to gain knowledge regarding overall device construction. Information learned serves as an invaluable aid toward device decapsulation, a process necessary to accomplish single-event effects (SEE) testing or failure analysis. Additional information regarding SEE testing can be found in a later discussion on PEM qualification.

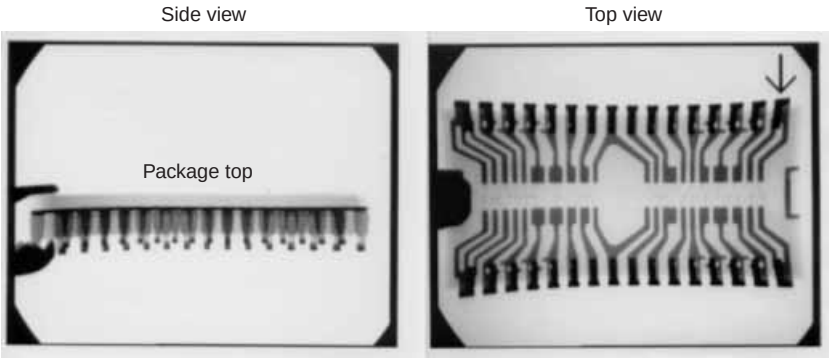

Figure 4. Real-time X ray of Samsung 64-MB dynamic random-access memory (DRAM) at ≈3.5X magnification. From the top view, the die occupies approximately 90% of the package, with the lead frame on the top.

Visual and Mechanical Inspection

Visual inspection is performed, on a 100% basis, in accordance with the nearest applicable standard (i.e., military, Joint Electronic Devices Engineering Council [JEDEC], best commercial practices, etc.). Mechanical inspection is performed, on a sample basis, in accordance with the same. The intent of these inspections is to ensure device compliance to purchase-order requirements.

PEM QUALIFICATION

Our approach to PEM qualification centers around a five-step testing regime:

1. Radiation hardness assurance
2. Temperature cycling
3. Steady-state temperature-humidity bias life test
4. Destructive physical analysis
5. High-temperature operating life

For reasons that will be outlined in the following discussion, all testing performed is considered to be destructive in nature. The specific tests chosen are designed to qualify PEMs for their mission environments, including integration, test, storage, transportation, launch, and mission life.

Radiation Hardness Assurance

All parts, commercial or military, must be evaluated for radiation hardness assurance (RHA). When required, testing is performed in accordance with MIL-STD-883, Method 5005, "Qualification and Quality Conformance Procedures," Group E, or its equivalent.

The Laboratory has found that total dose is not the main cause for concern for RHA. Most parts chosen either meet the low total dose requirements associated with the TIMED mission or can be adequately shielded against such effects. For PEMs, SEE testing can be cause for concern, specifically, the ability to decapsulate the PEM in order to perform the SEE test. (PEM decapsulation will be covered in more detail in a later discussion on destructive physical analysis.) With the advent of higher-energy charged-ion accelerators, it is no longer necessary to decapsulate every PEM to perform SEE testing. The limiting factor for these accelerators is the ability of the ion to penetrate through the plastic and into the active region of the die, which depends on the thickness of the package, passivation, and die.

When performing RHA testing, one must also compensate for the effects of burn-in. Data demonstrate that burn-in may impact radiation results.[12] As a result, parts used for RHA testing must resemble those in the flight configuration. If 100% burn-in is not performed as a screen, one must ensure that parts chosen for RHA testing are not burned in as well.

Temperature Cycling

The purpose of performing temperature cycling testing is to cull potential coefficient of thermal expansion (CTE) mismatches that occur when neighboring materials in the PEM expand and contract at different rates while being heated or thermally stressed. (Temperature cycling is only performed when adequate test data cannot be obtained from the device manufacturer.) Expansion and contraction cause shifts between the plastic, metal lead frame, and die surface. The typical failure modes associated with CTE mismatches are delamination, cracked passivation, cracked interlayer dielectric, metal line shifts, and cracked die.[2] Temperature cycling testing can induce or exacerbate these failure modes. Of key concern is delamination, which can aid corrosion by creating pathways for moisture ingress. Mitigating against the effects of delamination justifies the need to conformally coat PWBs, as outlined previously.

When temperature cycling is performed, APL follows the guidelines established in JEDEC Standard JESD-22-A 104, "Temperature Cycling."[13] After the completion of testing, final electrical measurements at the mission temperature extremes and ambient are taken. Finally, selected samples are subjected to destructive physical analysis (DPA).

As an alternative to preconditioning, all parts used for temperature cycling are assembled onto flight-like boards (e.g., same materials and manufacturer as flight boards) and conformally coated before testing. (Preconditioning, as defined by JEDEC Standard A 113-A, "Preconditioning of Plastic Surface Mount

Devices Prior to Reliability Testing,"[13] helps evaluate long-term part reliability by taking into account the impact of multiple solder reflow operations.) APL takes this alternative approach to assembling PEMs, which removes the need to conduct preconditioning and qualifies the intended flight application in the process. Figure 5 depicts a PEM mounted on a test board.

Steady-State Temperature-Humidity Bias Life Test

The purpose of 85/85 testing is to ensure that parts can survive in the uncontrolled, moisture-laden environment before launch. (As with temperature cycling, 85/85 testing is only performed when adequate test data cannot be obtained from the device manufacturer.) Specifically, variances in moisture and temperature during integration, test, transportation, and storage of the spacecraft must be addressed.

Once in the vacuum of space, moisture becomes a nonissue; moisture is immediately depleted upon entering the vacuum environment. Protecting the devices while still on the ground requires the maintenance of a "moisture-free" environment. As already stated, APL uses both dry boxes and conformal coating to minimize moisture. Dry boxes, by their very nature, are moisture free. Conformal coating will not eliminate moisture, but it will slow it down and possibly filter out some ionic species.

When 85/85 testing is performed, we follow the guidelines established in JEDEC Standard JESD-22-A 101, "Steady-State Temperature Humidity Bias Life Test."[13] Testing is done in a manner consistent with that of temperature cycling; the parts are assembled onto flight-like boards and conformally coated before testing. After testing, final electrical measurements at the mission temperature extremes and ambient are taken, and selected samples are subjected to DPA.

Destructive Physical Analysis

As with radiographic inspection, the purpose of DPA is to build a knowledge base of component construction technology. Attention focuses on the effects of temperature cycling and 85/85 testing on PEM reliability.

When DPA is performed, APL follows the guidelines established in MIL-STD-1580, "Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts," as applicable. Observations and measurements made during DPA are expected to aid in the establishment of uniform pass/fail criteria associated with scanning acoustic microscopy results (delaminations).

For further understanding of delamination phenomena, all samples are subjected to C-mode scanning acoustic microscopy before decapsulation.

Currently three methods of decapsulation are available: oxygen plasma etching; wet etching with either red fuming nitric and/or red fuming sulfuric acid; and thermomechanical means including grinding, heating, and breaking of the plastic encapsulation by force. Each method has associated advantages and drawbacks. Final selection of a particular method depends on the results desired (e.g., functionality, access to internal structures, etc.). Figure 6 is a photograph of a decapsulated Samsung 64-MB DRAM using red-fuming nitric acid.

High-Temperature Operating Life Testing

Burn-in is only performed as part of qualification testing on a sample size basis for two reasons, the first and foremost reason having to do with temperature-related concerns. As already stated, most PEMs are not rated to +125°C. As such, testing 100% of the parts beyond the manufacturer's absolute maximum ratings is not recommended. The other reason for performing burn-in is time: If one were to consider burn-in on a 100% basis—applying the Arrhenius equation, with an assumed activation energy of 0.7 V, a standard burn-in of 168 h at +125°C, extrapolated to +70°C—it would require 3272 h to complete!

We know that during thermal vacuum testing of the TIMED spacecraft some PEMs will exceed their data sheet temperature limits. As such, survivability of devices at these temperatures must be ensured. The purpose of carrying out high-temperature operating life (HTOL) testing, therefore, is to ensure long-term device reliability as well as to provide justification for uprating the components.

When HTOL testing is performed, APL follows the guidelines established in JEDEC Standard JESD-22-A 108, "Bias Life."[13] Dynamic bias is preferred, but not mandatory. The sample size for HTOL testing is 22 pieces. The time and temperature used are 1000 h and

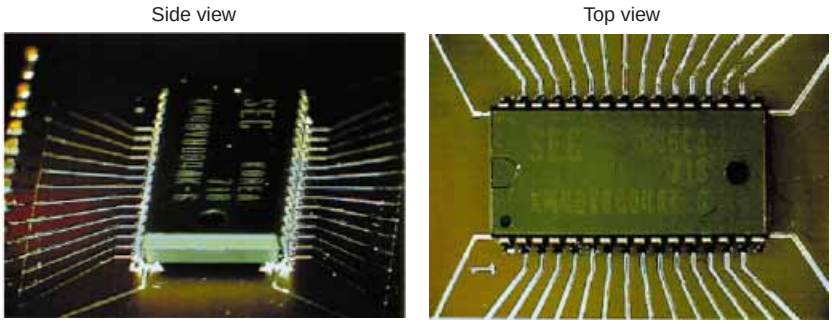

Figure 5. Samsung 64-MB DRAM mounted on a test board. Boards are manufactured with flight-quality material, and parts are conformally coated. This approach replaces the standard preconditioning method by simulating actual flight conditions.

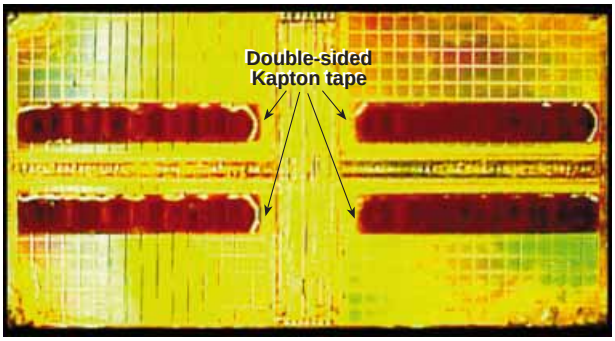

Figure 6. Top view of a Samsung 64-MB DRAM decapsulated using red-fuming nitric acid (intended use, single-event effects testing).

+125°C, respectively. Unlike thermal cycling or 85/85 testing, preconditioning and conformal coating are not needed. HTOL testing is concerned with "infant mortality" and long-term reliability of devices to withstand temperature extremes. At the completion of testing, final electrical measurements at the mission temperature extremes and at ambient are taken.

LONG-TERM DORMANT STORAGE

Although the relevance of this topic may not, at first, be readily apparent to our discussion, it does serve two beneficial purposes. First, as the heading implies, it is sometimes necessary to store a spacecraft, box, board, or piece-part for an extended amount of time before launch. We must therefore know that the PEMs will operate reliably after exposure to a variety of environmental stresses. Second, compared with the benign environment of space, knowing that PEMs can survive the rigors of long-term dormant storage provides additional justification for their use in spaceflight applications.

The qualification tests outlined previously concentrate solely on the individual effects of temperature and moisture on PEMs. Limited studies have been conducted on the so-called "wooden-round" concept, which concerns the synergistic effects of moisture and temperature on PEMs under uncontrolled, long-term dormant storage conditions.

The Laboratory has already completed one such study for the Navy's F/A-18 Program.[1] Ninety-two PEMs were involved in this effort, with parts dated as early as 1967. The results of the investigation revealed that only two devices, both 28 years old, exhibited evidence of corrosion. In addition, 91% of the parts were found to be delaminated. The low number of corrosion failures can be attributed to improvements in epoxy/novolac formulation. As for the high percentage of delamination observed, this provides justification for the use of conformal coating by APL.

Recently, the Laboratory was selected to be an independent assessor for the Army's Missile Command (MICOM). This study involves 16 PEM lots from 10 manufacturers, for a total of 160 pieces per lot (1600 pieces total). Each lot will be split into three groups of 50 parts, with three control samples per group, and subjected to the testing outlined in Fig. 7. The purpose of the study

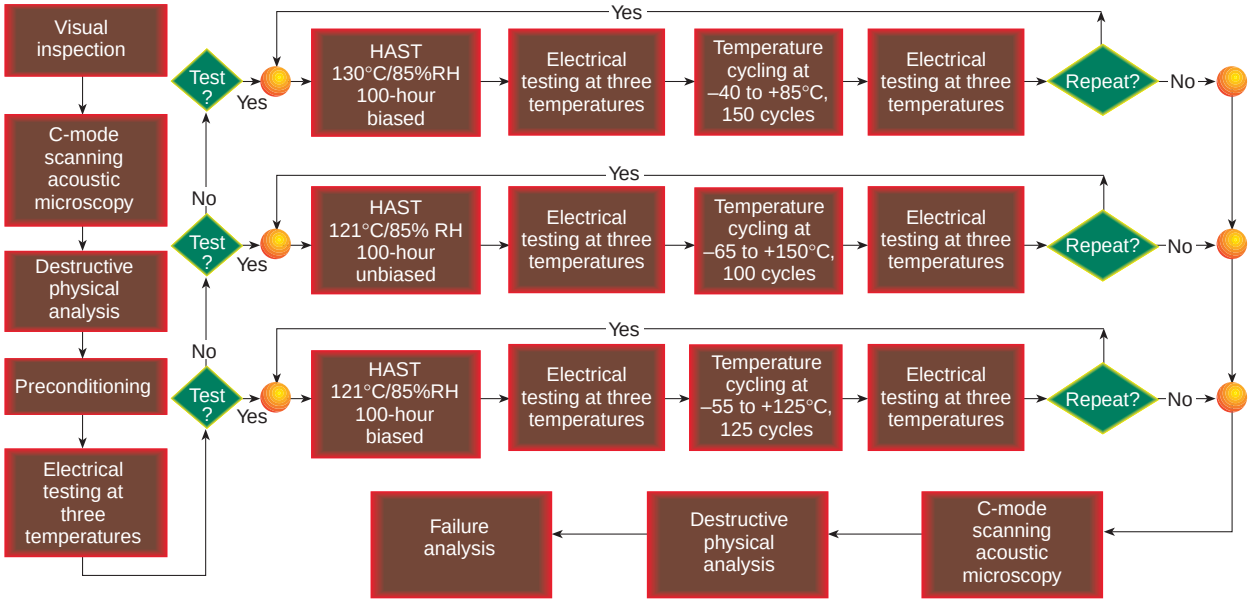

Figure 7. Diagram of APL's Army Missile Command study investigating the effects of multiple environmental stresses on PEMs (HAST = highly accelerated stress test).

is to gain further knowledge of the synergistic effects of temperature cycling and moisture on PEMs as related to long-term dormant storage issues. Based on the results of the F/A-18 study, of particular interest is the effects of these stresses in the presence of delaminations. To that end, both C-mode scanning acoustic microscopy and DPA testing are performed before and after application of any environmental conditioning.

SUMMARY

This article has demonstrated how APL has selected, screened, and qualified PEMs for use in the TIMED Program. Our approach is founded on the knowledge that the primary failure modes associated with PEMs are ground related (i.e., before launch). We have shown that the management of PEMs involves a concurrent engineering effort that begins with the establishment of partnerships with a few world-class suppliers and ends with the development, documentation, and enforcement of rigorous in-house controls regarding device handling, screening, qualification, uprating, de-rating, and storage. The TIMED solid-state recorder exemplifies the need for incorporating PEMs into future spacecraft designs, emphasizing that technological challenges facing today's spacecraft manufacturer can only be met through the effective use of these commercially available devices. Finally, we anticipate that our testing in the area of long-term dormant storage will expand the knowledge required to rationally and reliably use these devices in spaceflight applications.

REFERENCES AND NOTES

[1] Casasnovas, A., and White, J. W., "Commercial Plastic Encapsulated Microcircuits for Naval Aviation Applications," *Johns Hopkins APL Tech. Dig.* 18(1), 50–58 (1997).

[2] Nguyen, L. T., Lo, R. H. Y., Chen, A. S., and Belani, J. G., "Molding Compound Trends in a Denser Packaging World: Qualification Tests and Reliability Concerns," *IEEE Trans. Reliability* 42(4), 518–535 (Dec 1993).

[3] Pecht, M. G., Nguyen, L. T., and Hakim, E. B., *Plastic-Encapsulated Microelectronics: Materials, Processes, Quality, Reliability, and Applications*, John Wiley & Sons, New York (1995).

[4] Lantz, L. II, "Fundamental Studies in Plastic Encapsulated Microcircuits," in *Advanced Plastic Encapsulated Microelectronics Short Course*, CALCE Electronic Packaging Research Center, University of Maryland, College Park (Aug 1997). Note: The figure presented is the result of original ongoing research performed at the University of Maryland by the CALCE Electronic Products and Systems Consortium. The experiment was designed and executed by Mr. Leon Lantz II and Professor Michael Pecht. Please contact Dr. Pecht via e-mail at pecht@eng.umd.edu for further information.

[5] Ash, W. M. III, *High-Reliability Space Flight Application of Plastic Encapsulated Microcircuits: A Feasibility Study*, SOR-3-94009, JHU/APL, Laurel, MD (Feb 1994).

[6] Copies of documentation can be obtained by contacting The Institute for Interconnecting and Packaging Electronic Circuits (IPC) at (708) 677-2850 or visiting the IPC home page at http:\\www.ipc.org.

[7] Cooper, K., *Plastic Bag Study*, SOR-3-94088, JHU/APL, Laurel, MD (Oct 1994).

[8] Gardner, J. R., "The Appropriateness of Plastic Encapsulated Microcircuits in a Specific Wooden-Round Application," *IEEE Trans. Reliability* 45(1), 10–18 (Mar 1996).

[9] Condra, L., O'Rear, S., Freedman, T., Flancia, L., Pecht, M., and Barker, D., "Comparison of Plastic and Hermetic Microcircuits Under Temperature Cycling and Temperature Humidity Bias," *IEEE Trans. Components, Hybrids, Manuf. Technol.* 15(5), 640–650 (Oct 1992).

[10] Maurer, R. H., Le, B. Q., Nhan, E., Lew, A. L., and Garrison-Darrin, M. A., "Fabrication and Qualification of Coated Chip-on-Board Technology for Miniaturized Space Systems," in *Proc. 3rd ESA Electronic Components Conf.*, ESA SP-395, ESTEC, Noordwijk, The Netherlands, pp. 199–204 (Jul 1997).

[11] McCluskey, P., "Uprating: Introduction and Key Concerns," in *Electronic Component Management & Uprating Workshop*, CALCE Electronic Packaging Research Center, University of Maryland, College Park (Aug 1997).

[12] Shaneyfelt, M. R., Winokur, P. S., Fleetwood, D. M., Hash, G. L., Schwank, J. R., and Sexton, F. W., "Impact of Aging on Radiation Hardness," *IEEE Trans. Nucl. Sci.* 44(6), 2040–2047 (Dec 1997).

[13] Copies of documentation can be obtained by contacting The Joint Electronic Devices Engineering Council (JEDEC), which is sponsored by the Electronic Industries Association (EIA), at (703) 907-7558 or visiting the JEDEC home page at http:\\www.jedec.org.

THE AUTHORS

ANDREW F. MOOR is a senior staff engineer in APL's Space Department. He received his B.S. degree in engineering science in 1987 from Loyola College and an M.E.M. degree in engineering management from George Washington University in 1995. Mr. Moor previously worked at Unisys Corporation in support of various NASA Goddard Space Flight Center programs and Westinghouse Advanced Technology Labs in support of various DoD and NASA programs. He joined APL's Space Reliability and Quality Assurance Group in 1993 and is currently the lead component reliability and performance assurance engineer for several APL programs. He is a member of IEEE. His e-mail address is andrew.moor@jhuapl.edu.

ANTHONY CASASNOVAS received a B.S. degree in electrical engineering from the Instituto Technológico de Santo Domingo, Dominican Republic, in 1987 and a master's degree in engineering management from George Washington University in 1995. He worked at Unisys Corporation in Lanham, Maryland, in support of various NASA Goddard Space Flight Center programs before joining APL in 1994 as a senior component reliability and performance assurance engineer for the Space Reliability and Quality Assurance Group. Mr. Casasnovas is a member of IEEE. He is currently employed by Honeywell, Inc., Space Systems Division, Clearwater, Florida. His e-mail address is casasnovas@space.honeywell.com.

STANLEY R. PURWIN is a member of the Principal Professional Staff of APL's Space Department. He was awarded a B.Eng. in electrical engineering in 1966 from Stevens Institute of Technology, Hoboken, NJ, and an M.S.M.E. from Newark College of Engineering (now New Jersey Institute of Technology) and an M.B.A. from Rutgers University, both in 1970. He worked in electronics manufacturing at several Fortune 500 companies as quality manager, manufacturing engineering manager, and director of manufacturing before joining APL. Mr. Purwin is currently the supervisor of the Space Reliability and Quality Assurance Group. His e-mail address is stan.purwin@jhuapl.edu.