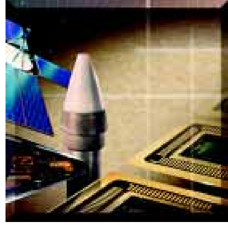

Miniaturization of Space Electronics with Chip-on-Board Technology

Binh Q. Le, Elbert Nhan, Richard H. Maurer, Robert E. Jenkins, Ark L. Lew, Howard S. Feldmesser, and Juan R. Lander

Miniaturization of space electronics by eliminating individual chip packages is attractive not only because of the advantage of reduction in both volume and weight but also because of the potential improvement in reliability associated with elimination of the first level of packaging at the chip. Most importantly, miniaturization can lead to significant cost saving in a space program since a smaller launch vehicle may be used. The APL study of chip-on-board technology began with the miniaturization of a magnetometer signal processor to verify the manufacturability of the new advanced packaging process. Subsequently, encapsulant-covered dynamic-random-access-memory test boards and triple-track chips were subjected to an environmental stress program to qualify the technology for flight. This article presents an overview of the chip-on-board technology: the approach, methodology, and test results and its significance and potential effect on the future direction of space programs.
(Keywords: Chip-on-board, Die coating, Direct chip attach, Electronics miniaturization, MCM-L.)

INTRODUCTION

Chip-on-board (COB) technology involves mounting bare dies directly on a substrate without the need for the component's package. Eliminating the component package reduces the required substrate area and assembly weight and removes one entire level of interconnects. The saving in area can be as much as 90% in some cases. Using conventional printed wiring boards (PWBs) and standard wire bonding technology, COB technology can yield a factor of at least 10 in weight and volume saving.[1] COB technology also reduces the thermal resistance and the number of interconnects between an active die and the substrate (i.e., the package pins), which can potentially improve the overall circuit speed and the reliability of the design.

In theory, there is no distinct difference between multichip module (MCM) and COB technologies. In practice, MCMs often use a smaller substrate and fewer active dies as compared with COB design. MCMs also require hermeticity in most cases, and this requirement

does not apply for COB design. Many companies support MCM technology. Major industrial consortiums have been formed under the auspices of the Defense Advanced Research Projects Agency in search of low-cost, quick-turnaround substrates for MCM technology.

The three major technologies for MCM are MCM-D, MCM-C, and MCM-L (-D, -C, and -L represent the different types of substrate materials). MCM-D provides substrate designs of the highest density since it uses thin film processes to deposit metals and dielectric layers on various rigid bases. MCM-C provides substrate designs of moderate density and uses thick film technology to form conductive patterns on ceramic materials. MCM-L uses laminate structures and employs PWB technology to form conductive patterns over reinforced dielectric laminates. Conventional PWB technology with an etching process can provide a feature size as small as 5 mil. With the development of the additive process in PWB technology, laminated substrates can achieve features as small as 3 mil. These characteristics, and its low cost, make MCM-L technology popular and attractive.

COB technology is very similar to MCM-L technology and has several advantages. It supports the use of both conventional soldered components and bare dies on a laminate dielectric substrate. It saves weight and volume compared to the conventional MCM technology with hermetic packages since it eliminates the intermediate substrate and pins of an MCM device. For a graphical comparison among the COB, MCM, and single-chip package technologies, see the article by Bevan and Romenesko, their Fig. 1, this issue.

APL SPACE DEPARTMENT MINIATURIZATION OBJECTIVES AND RELATED PROJECTS

In recent years, the ever-changing world political climate and the resulting shift in government policy to reduce spending have significantly cut the funding level for both NASA and defense space programs. DoD and NASA sponsors' requirement for "faster, better, cheaper, and now smaller" development for space missions underscored the need to miniaturize spacecraft. Recognizing the changes in process, the APL Space Department, in collaboration with the Technical Services Department, launched an internal research and development initiative in 1994 to make major improvements in our flight electronics. A component of that initiative was to introduce and space qualify a new packaging technology. COB was selected because of its many advantages over the other competing technologies. Once COB methods are space qualified, electronic subsystems on a spacecraft can be reduced by a factor of 10 in volume and weight. Miniaturized electronics could result in major cost reduction because of the use of smaller launch vehicles and multiple payloads on the same launch rocket. The COB qualification effort has led to two other projects currently under development: a miniaturized scientific imager (MSI) and a command and data handling in your palm (C&DH IYP) system.

1994 Study

During the first year, the study focused on rebuilding, with COB technology, an existing filter analog-to-digital (FAD) board assembly of a magnetometer signal processor. This board was selected because it was the most complex board design that included both digital and analog components. The objectives of the study were to bring to light and deal with all the COB challenges and to show that, even without an optimized electronic circuit redesign, the new packaging approach could provide significant weight and volume reduction. The project was also aimed at understanding the issues associated with rework of COB assemblies: how to minimize manufacturing cost and how to acquire, handle, and qualify unpackaged integrated circuits.

The FAD project objectives were achieved after several reworks and rebuilds. By eliminating device packages, the COB approach reduced the weight and volume of the FAD electronics by almost an order of magnitude.[2] The only changes introduced in the FAD design were the use of COB and three-dimensional (3-D) modular packaging methods to mount the components. Figure 1 provides a comparison between the original Freja magnetometer signal processor design and the new design with COB.

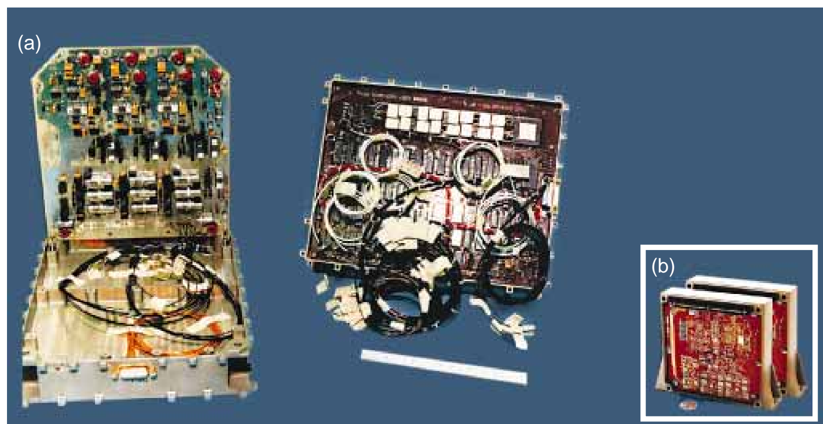

Figure 1. The Freja magnetometer signal processor. (a) Original design: Size = 9.8 × 7.9 × 3.54 in.; weight = 6.7 lb. (b) COB design: Size = 4.5 × 4.5 × 2 in.; weight = 1 lb.

1995 Study

In the second year of the COB project, from the results of our initial work, the evaluation of die coating material was our main focus. The coating encapsulant provides protection for bare dies during manufacturing and handling and throughout all flight environments. The selected coating had to be reworkable to ensure the viability of low-cost satellite electronic designs. Several candidate materials were selected based on the results of years of extensive research in the automotive, military, communications, computer, and space industries.

A dynamic-random-access-memory (DRAM) test board with a 3-D stacked DRAM module from Irvine Sensors as shown in Fig. 2 was used to support this study. The 3-D stacked DRAM module consists of six layers of individual dies and an aluminum nitride top layer that includes a wire-bondable top surface. Intermediate thin film–deposited layers located on top of each die provide interconnection from the die bond pads to the edge circuitry. This edge circuitry brings all connections to the bond pads located on the top side of the module. The 3-D memory modules use five of the 16-Mbit DRAM dies, with one being a spare, for a total memory capacity of 80 Mbit. The extra die helps improve the final yield by allowing the manufacturer to reselect five good dies out of the six available after completion of the module lamination process. This technique greatly improves the final yield of the module. Using this structure miniaturizes electronic hardware since it occupies the otherwise wasted area in the vertical direction.

1996 Study

In 1996, environmental testing—which included a dynamic loads test, a temperature cycling test, and a temperature–humidity bias (THB) test at 85°C and 85% relative humidity (85°C/85%RH)—was performed to evaluate the reliability of COB technology for long-term satellite applications. Because the space environment is devoid of moisture, the 85°C/85%RH THB test is not directly applicable. However, since COB flight hardware will be extensively handled during design and testing on the ground, a suitable die encapsulant is required to provide protection from the surrounding environment.

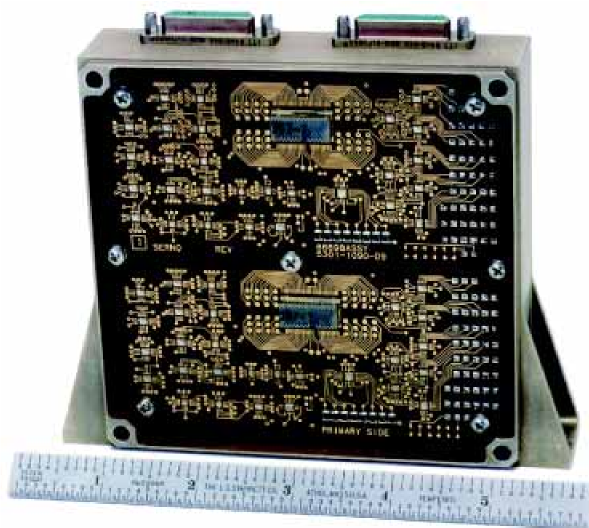

Figure 2. Photograph of a dynamic-random-access-memory board.

1997 Study

The COB effort during 1997 was focused on the detailed manufacturing processes and standards via the development of the MSI and the C&DH IYP systems. The ultimate success of COB technology will rest upon the successful implementation of the advanced packaging technology on these two systems.

CHIP-ON-BOARD DEVELOPMENT APPROACH

In addition to the potential overall program cost saving, there are several other advantages to developing COB-based space hardware. Once a well-controlled process is established, COB fabrication costs can be controlled and minimized compared with standard MCM technology with hermetic packages. The lower fabrication cost is a result of elimination of the first level of packaging (chip package). Since the COB packaging technique in this study is based mainly on populating bare dies on a suitable multilayer laminate substrate that is not hermetically sealed, die coating for protection from the environment is required. In recent years, significant improvements have been made in die coating materials. Epoxies, silicone, Parylene, and silicon nitride are desirable because of their low coefficients of thermal expansion (CTEs) and good moisture-resistant capability.

Since the interconnection interface is usually the weak link in a system, the overall COB circuit or system reliability may actually be improved because one entire level of interconnect and packaging at the chip has been eliminated. With COB, mixing of packaging technologies is also possible. Because some devices are available only in commercial plastic packages, populating a multilayer laminate substrate with both bare dies and plastic-packaged parts is inevitable. In COB design, it is possible to rework the chip, if necessary, if die coating is applied only on the die top. This method allows replacement of individual dies that are found to be defective instead of replacement of the entire board. In terms of thermal management, COB devices offer a shorter thermal resistance path than their packaged counterparts, and their shorter signal paths also enhance circuit performance.

Implementing COB technology requires some changes from the current processes used with packaged parts. It demands a controlled environment to avoid problems resulting from handling that may cause damage to the bare dies and the wire bonds interconnecting them. A controlled environment entails many standard items that are being used at APL for actual flight hardware, such as protective covers for COB assemblies, controlled ambient conditions for die storage purged with dry nitrogen, protective clothing for personnel, electrostatic discharge protection, and laminar flow work benches. COB technology with wire bonding relies heavily on existing hybrid technology that is supported by numerous vendors and the Technical Services Department at APL.

DESIGN AND FABRICATION DETAILS

The four major COB technology components and processes—known good die, PWB technology, die attach technology, and die coating—are described next.

Known Good Die

Success in COB design and manufacture starts with fully tested die, or known good die. The COB or MCM yield depends on the chip yield and the number of chips in the design. In theory, the statistical yield of a COB assembly Y_m versus the chip yield Y_c and the number of chips N_c is given by the equation

$$Y_m\ (\%) = 100\ (Y_c)^{N_c} .$$

This equation gives only the theoretical yield of the COB assembly without considering the maturity of the die technology and the rework variables. Figure 3 shows the probability of the theoretical yield of COB or MCM assemblies plotted against die yield. Testing of individual dies is very difficult because of the small size of the features associated with bare dies. However, recent industry studies reveal that the yield for common components such as static random-access memory, DRAM, and medium-scale integrated circuits can exceed the 99.5% level. The reworkability of COB technology would also increase the potential yield of the final assembly.

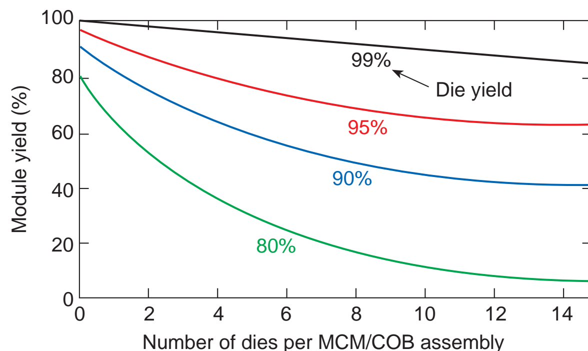

Figure 3. Effects of known good die on yield of COB or MCM assemblies.

PWB Technology

Many different types of substrate materials can support COB technology. Typical PWB materials are FR4 epoxy/glass, polyimide/glass, polyimide/quartz, BT/glass, cyanate ester/glass, and polyimide/Kevlar. FR4 is by far the most commonly used resin material in the electronics industry. However, because of FR4's low glass transition temperature, polyimide/glass material is preferable for high-reliability and thermosonic wire bonding applications. The glass transition temperature is the temperature at which the phase of the material changes to a gel-like substance. During this phase change process, the CTE can increase by an order of magnitude, which may impose excessive thermal stresses on dies and other onboard components.

Other important factors to consider in selecting a suitable PWB technology include the compatibility of the CTEs of the board and the dies and the water absorption of the board material. Polyimide/Kevlar material, although exhibiting a better CTE compatibility than other PWB materials, has a high water absorption characteristic. This undesirable feature makes the board more difficult to clean. Cyanate ester resin with glass reinforcement seems to be the most desirable material, with excellent characteristics in water absorption, CTE, and dimensional stability. However, it is the most expensive PWB material, it is extremely difficult to work with, and there are very few vendors who can support this technology. Polyimide/glass PWB material was, therefore, selected for the COB study.

Die Attach Technology

The choice of die attach technology is an important consideration when examining the option of using dies in a design. There are many techniques for die attachment and interconnection, but the two most common techniques are wire bonding and flip chip, commonly embodied as the controlled-collapse chip connection. Flip-chip die bonding requires that solder bumps be placed on the die's bond pads. In this process, the die is placed on the PWB with the integrated circuits' metallized pattern facing the board. The solder bumps are then reflowed, providing both mechanical and electrical connection to the PWB. During the solder reflow process, surface tension of the solder material provides self-alignment of the die with respect to the PWB, removing any alignment mismatch created during placement of parts. The advantage of this process is that

it can significantly increase the number of package pins from the die without increasing the die area.

A low-stress underfill material is injected underneath the die to strengthen the attachment of the die to the board and reduce the thermally induced stress to the solder joints. The underfill material also provides a seal that protects the die from the environment. However, reworkability, inspection, die availability, and manufacturing difficulties are barriers for this die attachment process.

There is another version of the controlled-collapse chip connection process that uses conductive epoxy instead of solder.[3] This process requires, typically, gold bumps on the die pads. It provides no self-alignment, but the attachment induces little stress because of the lower temperatures used. However, not many operations support this process either.

For wire bonding, the die is attached directly to the PWB on its back side and electrical connection is made using bond wires. The bond wires can be made of aluminum or gold. The process is very similar to that used when placing dies in standard chip packages, hybrids, and MCMs. As a result, many companies have standard production lines in place that can support wire bonding assemblies. The wire bonding process does not impose additional thermal stresses on the bond wires. The wires are self-supported at both ends. This process allows for visual inspection, the nondestructive pull test, and rework. Most dies are available in a form that supports a wire bond process.

Die Coating

All bare dies have a thin layer of passivation of SiO_2, Si_3N_4, or polyimide material that covers the circuit to provide protection from the environment, with the exception of the bond pads. This passivation is done by the integrated circuit foundry at the wafer stage. It requires high temperature and accurate application thickness. Since the bond pads are made of aluminum, they can easily corrode if they are not protected. Therefore, coating materials are extremely important in COB technology. The material of choice must be compatible with the soldering assembly process since COB technology is often mixed with surface-mount technology. The material should have a CTE similar to that of the bond wire material and a glass transition temperature beyond the expected operating environment to avoid high thermal stresses. The material must adhere well to the die surface with minimum void and have low ionic content to minimize the possibility of corrosion. Five major criteria for selecting the die coating material are as follows:

1. CTE close to that of the wire material (gold wire has a CTE = 14.2×10^{-6} m·m^{-1}·°C^{-1})
2. High glass transition temperature
3. Low cure shrinkage
4. Void-free fill over wires and die
5. Low ionic contamination content (<20 parts per million Na^+, K^+, Cl^-)

Silicone

Silicones and epoxies are two major groups of die encapsulant materials. Silicone is a gel-like material. It offers low alpha particle emission, high purity, and low modulus of elasticity. Silicone also has very low ionic content and a low water saturation level. On the negative side, silicone's inherently high CTE can cause excessive thermal stresses on wire bonds during temperature cycling. Dow Corning HIPEC Q1-4939 silicone was used in our tests (Table 1).

Epoxy

Epoxy is a class of polymers with low ionic content, a high glass transition temperature, and a high modulus of elasticity. The epoxy candidate must have a low CTE that is comparable with that of gold wire bonds, and it provides excellent mechanical protection. Dexter Hysol FP4402 and FP4450 epoxies were used in our tests (Table 1).

Silicon Nitride

Silicon nitride coating applied at room temperature is a proprietary process developed by Ionic Systems, Inc. It is a plasma-enhanced chemical vapor deposition process. Unlike the conventional silicon nitride deposition in wafer manufacturing, which requires a high temperature, this process deposits a uniform inorganic coating on silicon dies in COB assemblies at room temperature. It provides excellent protection against moisture owing to its extremely low moisture permeability. Table 2 compares the permeability of silicon nitride and other die-coating materials.

Table 1. Mechanical properties of select encapsulants.

Material	CTE (m·m^{-1}·°C^{-1})	T_g (°C)	Na^+, K^+, Cl^- (ppm)
Hysol FP4450 epoxy (Dexter)	19×10^{-6}	157	2, 3, 5
Hysol FP4402 epoxy (Dexter)	22×10^{-6}	155	<20, 20, 20
HIPEC Q1-4939 silicone (Dow Corning)	105 to 262×10^{-6}	NA	2, 2, 0

Data are from the manufacturers' specifications.
Note: NA = not available; ppm = parts per million; T_g = glass transition temperature.

Table 2. Permeability of various die-coating materials.

Material	Moisture permeability ($g \cdot m^{-2} \cdot 24\ h^{-1}$)
Silicone nitride	<0.00465
Parylene C, D	3.26–3.88
Parylene N	23.25
Epoxides	27.75–36.89
Urethanes	37.20–134.85
Silicones	68.20–122.45

Parylene

In the COB study at APL, Parylene C was used. It is a white crystalline solid with a high melting point that provides a uniform conformal coating for electronic assemblies. Parylene is a chemically and mechanically stable material. It is insoluble in all organic solvents up to 150°C and resists permeation by all solvents except for aromatic hydrocarbons. Typical applications of Parylene coating have a thickness of about 1 mil. The application process is a vapor deposition that applies a uniform coating in a free molecular mode under vacuum.

TEST VEHICLES

Three different test vehicles were used in this study: the FAD board, DRAM board, and triple-track chip.

FAD Board

A magnetometer signal processor that was flown on the Freja spacecraft was selected for the miniaturization experiment. The entire electronic assembly is composed of three separate subsystems: the front-end sensor electronics, the FAD board, and the processor board. To effectively demonstrate the manufacturing viability of COB packaging technology, a FAD circuit board was fabricated using the new approach. The FAD board was chosen because of its relative circuit complexity compared with the other two boards. The FAD circuit design incorporated analog, digital, and mixed signal circuitries and integrated circuit complexity ranging from discrete to very-large-scale integrated technologies using different power supply voltages.

The COB substrate design consists of two 8-layer boards mounted in a magnesium housing, with an elastomeric connector providing interconnection between the boards. The board design used 5-mil lines and spacings to provide high-density routing. The conductors on the outer layers had electrolytic nickel and gold plating. The nickel layer provided a diffusion barrier between the gold and the copper layers to prevent the formation of the intermetallic (Au-Cu) compound that often causes bond wire failure. The thermosonic process used heat along with ultrasonic energy to create the bond.

The COB FAD design (Fig. 1b) was successfully employed, resulting in a size and weight reduction by almost an order of magnitude. Electrical performance of the FAD board was verified with existing test equipment after the debugging and repair process was completed.[2]

DRAM Board

The second test vehicle was a DRAM board (Fig. 2). The basic function of this circuit is to continuously and completely exercise the 3-D stacked DRAM module with a memory capacity of 80 Mbits. The module consists of six DRAM die layers stacked on top of one another to form a 3-D rectangular cube. The DRAM module contains 4 million 4-bit-wide memory address locations. Upon power-up, the circuit becomes fully functional with an externally applied system clock and eight pattern lines. The pattern bits are shifted at the rising edge of each system clock to provide a different data pattern to each memory location, upon which four distinct operations—refresh, write, refresh, and read—are performed. Each address location in the DRAM module is accessed every 4,194,304 clock cycles.

Triple-Track Chip

The triple-track chip is a special test device designed to detect corrosion. Version 01 test chips provided by Sandia National Laboratories were used to complement this COB coating study. These test chips contain two types of test structures: triple-track and ladder. Triple-track structures consist of very closely spaced, parallel aluminum tracks in triplets that run in a serpentine pattern. The resistance of each track can be measured and monitored for detecting corrosion. The leakage current between the tracks can also be measured to monitor any conducting path formed by ionic contaminants, dendritic growths, or other corrosive agents. To characterize corrosion-induced failures quantitatively, ladder structures are available. A ladder consists of a number of aluminum conductor tracks connected in parallel between two wide metal bus bars. As the individual conductors open as a result of corrosion, the overall ladder resistance increases in a stepwise fashion. There are several triple-track and ladder test structures on each die. The substrate of a triple-track die is made of oxide-coated silicon. Some triple-track dies are passivated with a 7000-Å silicon nitride capping layer, whereas others are unpassivated.

Fifteen passivated samples and an additional 15 unpassivated samples—coated with various combinations of Parylene/FP4402, FP4402, Parylene/FP4450, FP4450, Parylene/silicone, silicone, and Parylene die-coating

materials—were packaged in 40-pin dual-in-line lead frames (see Fig. 4 for details and Table 3 for the test matrix). Additional samples without any coating were also included in this test to serve as controls. For the temperature cycling storage test, the parts were unbiased while inside the environmental oven. However, for the 85°C/85%RH THB test, the devices were powered to accelerate corrosion. The triple-track structures were biased at 5 V from the exterior track to the middle track and at –5 V from the interior track to the middle track. For the ladder structures, one ladder on each test chip was biased at 5 V across the pads while the other one was at –5 V.

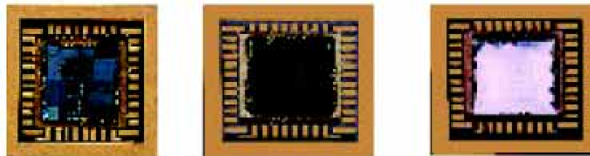

Figure 4. Photograph of the triple-track devices inside a 40-pin dual-in-line package.

TEST ENVIRONMENTS

We wanted to qualify the coated COB technology for space application and also to determine which

Table 3. Triple-track coating and environmental test matrix.

Sample no.	Die passivation	Die coating: 1st coating	Die coating: 2nd coating	Test	Note
1	No passivation	FP4450[a]	No coating	85/85[b]	
2	No passivation	FP4450	No coating	85/85	
3	No passivation	FP4450	Parylene	85/85	
4	No passivation	FP4450	Parylene	85/85	
5	No passivation	FP4402[c]	No coating	85/85	
6	No passivation	FP4402	No coating	85/85	
7	No passivation	FP4402	Parylene	85/85	
8	No passivation	FP4402	Parylene	85/85	
9	No passivation	Silicone[d]	Parylene	85/85	Top coat only
10	No passivation	Silicone	Parylene	85/85	Top coat only
11	No passivation	Silicone	No coating	85/85	Top coat only
12	No passivation	Silicone	No coating	85/85	Fill cavity
13	No passivation	Parylene	No coating	85/85	
14	No passivation	Parylene	No coating	85/85	
15	No passivation	No coating	No coating	85/85	
16	7000 Å SiN	FP4450	Parylene	85/85	
17	7000 Å SiN	FP4450	Parylene	85/85	
18	7000 Å SiN	FP4402	Parylene	85/85	
19	7000 Å SiN	FP4402	Parylene	85/85	
20	7000 Å SiN	Silicone	Parylene	85/85	Top coat only
21	7000 Å SiN	Silicone	Parylene	85/85	Top coat only
22	7000 Å SiN	Parylene	No coating	85/85	
23	7000 Å SiN	No coating	No coating	85/85	
24	7000 Å SiN	FP4450	Parylene	Temp. cycling	
25	7000 Å SiN	FP4450	Parylene	Temp. cycling	
26	7000 Å SiN	FP4402	Parylene	Temp. cycling	
27	7000 Å SiN	FP4402	Parylene	Temp. cycling	
28	7000 Å SiN	Silicone	Parylene	Temp. cycling	Fill cavity
29	7000 Å SiN	Silicone	Parylene	Temp. cycling	Top coat only
30	7000 Å SiN	Silicone	Parylene	Temp. cycling	Top coat only

[a]Dexter Hysol FP4450 epoxy.
[b]85°C/85%RH temperature–humidity bias test.
[c]Dexter Hysol FP4402 epoxy.
[d]Dow Corning HIPEC Q1-4939 silicone.

coating offered the most environmental protection. We used an environmental stress sequence of vibration followed by temperature cycling for qualification; to evaluate contamination and moisture protection, we used the conventional 85°C/85%RH THB test.[4] Electrical functionality tests were performed before, at intervals during, and after environmental stress on the Sentry-15 automatic tester. The Sentry-15 is a comprehensive automatic test system for characterizing very-large-scale integrated circuits and other digital components.

The dynamic loads envelope used is representative of a spectrum of launch vehicle environments for various past space programs at APL.

Thermal cycling was carried out in an environmental chamber for 1000 cycles. The temperature controller of the oven was set such that the test boards achieved a cooling and heating rate of between 10 and 12°C per min with a dwell time of 10 min at –55°C and 15 min at 125°C. Electrical functionality was verified on the Sentry tester at intervals of 100, 250, 500, 750, and 1000 cycles.

The 85°C/85%RH THB stress test was conducted in a temperature–humidity chamber for 1000 h. Test boards were mounted on a flat aluminum plate with the wire bond side exposed to the environment. A power supply external to the chamber provided bias voltage of –5 and +5 V applied to the boards through cables. The interior chamber temperature, the power supply voltage, and the current of each board were periodically monitored by a data logger. At intervals of 100, 250, 500, 750, and 1000 h, the specimens were removed from the humidity chamber. After a moisture bake-out inside another chamber, the boards underwent an electrical functionality test at 0, 25, and 85°C on the Sentry tester.

TEST RESULTS

DRAM Board

For the 11 test COB DRAM boards, all but one coating combination passed the vibration test. The lone failure, Parylene/silicone, was functionally intermittent. The same boards that underwent vibration testing were temperature cycled. The two samples of the Parylene/silicone/Si_3N_4 combination were completely nonfunctional after just 80 and 100 cycles. At 280 cycles, the Parylene/silicone circuit failed all electrical functionality tests. Five of the 10 samples completely passed electrical tests after 1000 cycles. The successful combinations were FP4450/Si_3N_4, Parylene/Si_3N_4, Parylene/FP4450, and Parylene/FP4402.

Nine coating combination samples were used in the 85°C/85%RH THB test. The control sample with no coating was completely nonfunctional after 150 h, as was the Parylene/Si_3N_4 combination. All die layers failed electrical functionality for the circuits covered with Si_3N_4 only and with silicone/Si_3N_4. The Parylene/silicone sample had a bad die layer at 150 h but otherwise remained mostly functional at 1000 h. The only coating combinations that successfully completed the 85°C/85%RH THB test were Parylene/FP4402, Parylene/FP4450, and FP4402/Si_3N_4.[5]

Triple-Track Chip

Final results from the temperature cycling test indicated that all coating combinations with Hysol epoxies successfully completed 1000 cycles. This was not the case for the silicone-coated dies. High thermal stresses resulting from the CTE mismatch between the encapsulant and the wire bonds caused some wire bond failures. Open circuits started to occur at 250 cycles, and the number of wire bonds that failed increased as the test progressed. The silicone results for the triple-track chips are consistent with those for the DRAM boards. Tables 3 and 4 summarize the test matrix and results, respectively, and Fig. 5 shows a broken wire bond in the heat-affected zone on a silicone-coated die.

Table 4. Temperature cycling test results (percent failed) for triple-track chips.

Die coating	No. of cycles 100	250	500	750	1000
FP4402 epoxy	0%	0%	0%	0%	0%
FP4450 epoxy	0%	0%	0%	0%	0%
Silicone	0%	17%	57%	81%	86%

Figure 5. Photograph of a broken wire bond on a silicone-coated die.

THB Test Results on Passivated Samples

Results from the 85°C/85%RH THB test indicate that for dies prepassivated with silicon nitride at the integrated circuit manufacturer, all samples coated with Hysol FP4402, FP4450, HIPEC Q1-4939 silicone, or Parylene completed the 1000-h test without any problem. The control samples without encapsulant failed starting at 250 h. Details of the test results are included in Table 5.

THB Test Results on Unpassivated Samples

In the 85°C/85%RH THB test, for samples without the manufacturer-deposited passivation, all but one die coating material (Parylene/FP4402) showed corrosion-related failures. The control samples that did not have any encapsulant protection completely failed shortly after the test started. Figure 6 summarizes the results of this test. A scanning electron microscopy inspection revealed widespread corrosion on the die surface and on the bond pads, causing open circuits and lifted wire bonds, as shown in Fig. 7. Energy dispersive spectroscopy also found evidence of carbon residues on the die surface.[6] The carbon traces were most likely the result of combustion of the die surface metallization under localized extreme thermal runaway conditions. (Thermal runaway phenomena are characterized by out-of-control temperature deviation from the normal operating temperature conditions.) Moisture and contaminants on the surface of unpassivated dies combined to result in corrosion.

Table 5. 85°C/85%RH test results (percent failed) for passivated dies.

Die coating	No. of hours 250	500	750	1000
Hysol FP4402/ Parylene	0%	0%	0%	0%
Hysol FP4450/ Parylene	0%	0%	0%	0%
HIPEC Q1-4939/ Parylene	0%	0%	0%	0%
Parylene	0%	0%	0%	0%
No coating	44%	44%	46%	75%

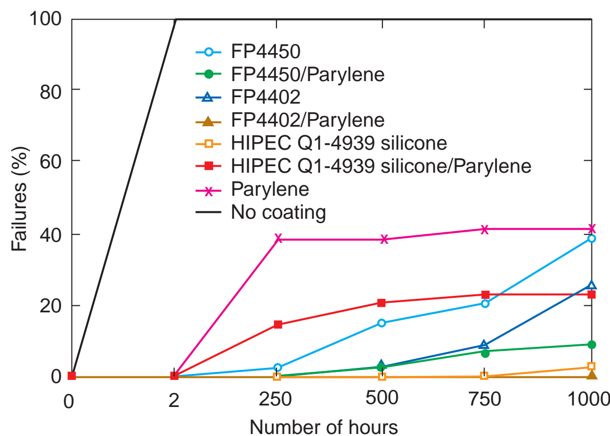

Figure 6. 85°C/85%RH test results for unpassivated dies.

SYSTEMS IN DEVELOPMENT

Miniaturized Scientific Imager

The MSI (Fig. 8) is a low-power, low-cost, multipurpose imager using COB technology and custom low-power application-specific integrated circuit devices. The complete system weighs less than 1.1 lb and has a maximum power consumption of 1.9 W. It is a flexible, highly integrated camera with a miniaturized

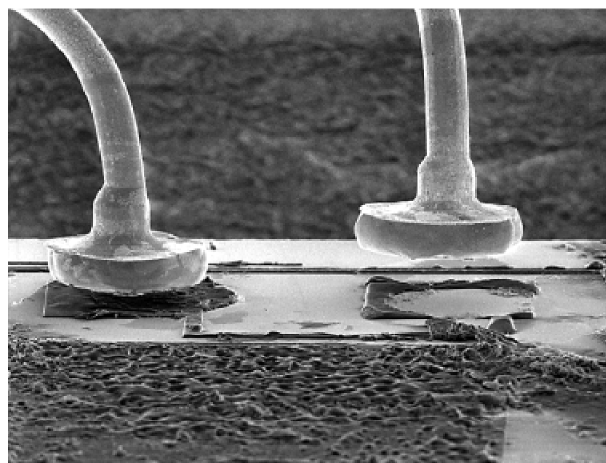

Figure 7. Scanning electron microscopy photomicrograph of a severely corroded die.

Figure 8. The miniaturized scientific imager. (a) Original design: Total weight = 17.5 lb (sensor = 8.5 lb, digital processor unit = 8.2 lb, harness = 0.8 lb). (b) COB design: Total weight of sensor and control electronics = <1.1 lb.

electronics module mounted directly to the optics.[7] The electronic design can be easily modified or customized for specific mission science objectives. This design does not have a Sun baffle since it is mounted inside the spacecraft; however, an external light baffle can be added to the existing design.

The MSI captures and stores an image in 1 of 32 defined memory locations upon command from the spacecraft. The MSI shutter speed and image memory location are selected via uplink command messages. An automatic gain control mode can be activated to override the selected shutter speed and permit the imager to autonomously select the appropriate shutter setting. The detector is an 8.8×6.6 mm charge-coupled device camera operating in the spectral range from 500 to 1000 nm. It is equipped with a low-power sleep mode to help improve spacecraft energy balance conditions while retaining stored images. The MSI powers up in the sleep mode and can be commanded into or out of that mode at any time. The imager downlinks the selected recorded image over its interface with the satellite data system upon receiving the appropriate command from the spacecraft. Each image consists of 1.5 Mbits of data. All imager downlink data formats include a 48-bit imager status word that contains critical imager diagnostic data.

Command and Data Handling In Your Palm

In a cooperative effort between the APL Space Department and the Goddard Space Flight Center Code 310 Assurance Technology Division, a family of miniaturized, stackable electronics modules is under development. These modules can implement anything from a stand-alone instrument processor to a C&DH system to the entire electronics needed by a spacecraft.[8] The small size of the modules makes them ideal for use in small satellites.

The C&DH IYP uses COB packaging technology developed at APL to implement a modular, expandable, generic spacecraft avionics system. The goal of this project is to develop and qualify a critical spacecraft electronics subsystem with a 10-fold reduction in size and weight over existing designs. The C&DH IYP has a volume of $4 \times 4 \times 1$ in. and weighs about 0.75 lb. Currently under development are a solid-state recorder module, an RTX2010 processor and interface module, and a Mongoose V processor and interface module. Technologies in the C&DH IYP include the following:

- COB packaging
- 3-D packaging
- APL-developed IEEE-1394 serial bus interface chip for intermodule communication
- Wireless infrared communication for test
- Reed-Solomon block code in the solid-state recorder
- Stacked memory
- Snapstrate mounting for testing and programming field-programmable gate array dies*

CONCLUSION

The FAD redesign project indicated that COB technology was completely compatible in functionality with the original Freja magnetometer signal processor electronics design, with a reduction in size of almost an order of magnitude. The reliability of COB technology is not assured, however, until a die-coating material is flight qualified. The DRAM and triple-track experimental projects emphasized the importance of the integrity and compatibility of the coating material in COB design. The candidate coating material must successfully complete vibration, thermal cycling, and 85°C/85%RH THB testing. Both Parylene/FP4450 and Parylene/ FP4402 die-coating combinations have been found to pass all these environmental tests. The finding is not surprising considering the track record of the encapsulant in the industry and its wire bond–compatible CTE.

The study has also shown that COB design is flexible since it supports both bare dies and packaged parts and, most importantly, rework on flight hardware. COB technology offers a potentially reliable and low-cost packaging approach to miniaturize flight electronics once the processes are qualified.

The prototype spaceflight systems, an imager, and a C&DH system are being developed.

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* A snapstrate is an adapter substrate that allows individual dies to be tested and programmed in a conventional socket. The substrate is much larger than the die in size. When the test is completed, unused areas on the substrate are broken away to leave a small portion of the substrate with a die mounted on top for the next assembly. Lockheed Martin Co. in Florida developed this design.

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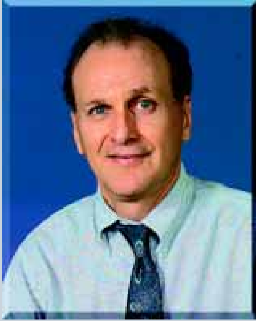

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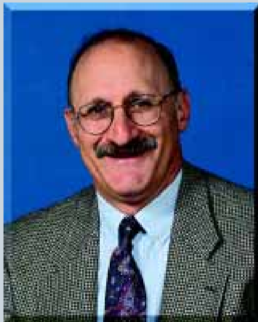

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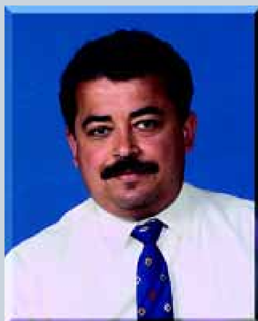

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