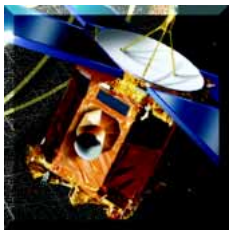

Data Processing Hardware for the NEAR Instruments

Christopher B. Hersman, John D. Boldt, Peter Eisenreich, Stephen F. Oden, and Deanna K. Temkin

By using a modular approach and common board designs, the Near Earth Asteroid Rendezvous (NEAR) program saved valuable resources in the development of data processing units for the instruments. The system is based on the Harris RTX 2010RH processor and includes a MIL-STD-1553B bus interface. The design uses a processor expansion bus to provide flexibility for the installation of custom boards supporting unique instrument interfaces.
(Keywords: Instrument data processing, Spacecraft computer, Space-qualified hardware.)

INTRODUCTION

On the Near Earth Asteriod Rendezvous (NEAR) spacecraft, many of the instruments are controlled by data processing units (DPUs), which respond to commands and process instrument data. The DPUs perform several tasks such as scheduling observations and performing data compression.

By developing a modular DPU, common hardware designs were used in multiple systems to meet the requirements of four of the NEAR instruments: the Multispectral Imager (MSI), the X-Ray/Gamma-Ray Spectrometer (XGRS), the Near-Infrared Spectrometer (NIS), and the Magnetometer (MAG). In addition to sharing common hardware designs, the requirements of the NIS and the MAG allowed these two instruments to share the same DPU.

DATA PROCESSING UNIT DESIGN

During the DPU design phase, the requirements of the four instruments were organized into common and unique functions. Common functions included onboard processing, interfacing with the spacecraft MIL-STD-1553B bus, and monitoring various analog sensor signals. The MSI and XGRS both required stepper motor control circuitry, and the MSI needed internal storage of 1.6 megabytes (MB) for image data. The specific data and control interfaces to each instrument were unique.

After identifying the common and unique functions, the system was designed so that the common functions were located on common boards that could be easily interfaced through a generic expansion bus to other boards implementing unique functions. This approach provided a modular design that could be expanded to meet the requirements of each instrument.

Figure 1 shows the division of functions between the boards in the MSI DPU. All three DPUs of the NEAR instruments shared the same designs for the power motor board, the RTX processor board, the 1553 board, and the analog input board. Although the instrument input/output (I/O) board and instrument power board were unique designs, all three DPUs contained boards

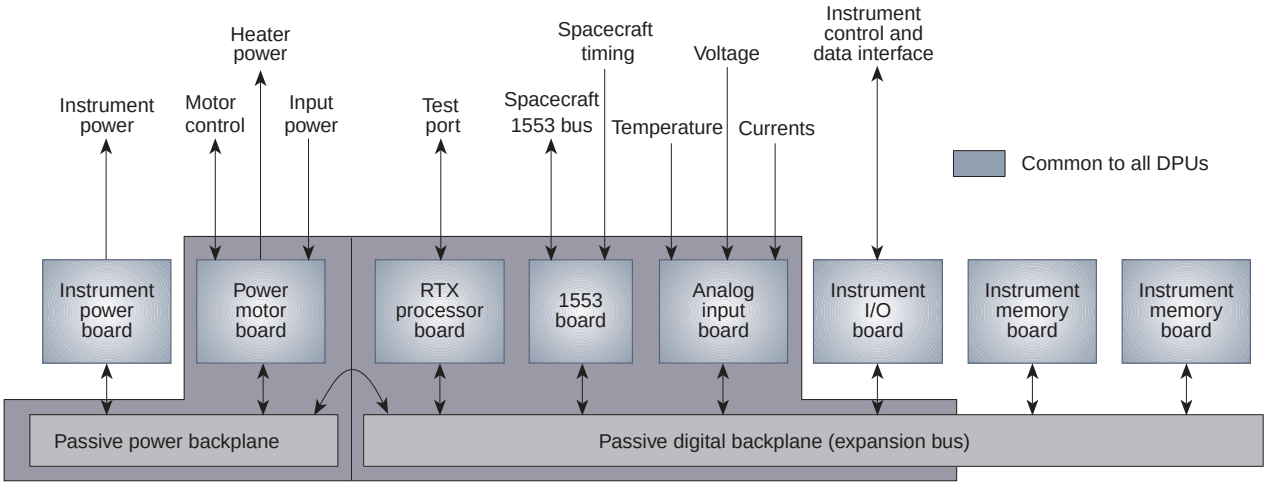

Figure 1. MSI DPU board configuration.

to perform these functions. Because the MSI needed a large amount of internal data storage, it contained two additional memory boards. Detailed descriptions of each board follow.

RTX Processor Board

The RTX processor board uses a Harris RTX 2010RH processor running at 6 MHz for the computing core. The board is equipped with 4K words of programmable read-only memory (PROM), 96K words of random access memory (RAM), and 32K words of electrically erasable PROM (EEPROM). The processor board also has access to additional resources through the expansion bus. A block diagram of the RTX processor board is shown in Fig. 2. Other important features include a watchdog reset, four edge or level sensitive interrupts, a low-voltage reset circuit, and an EEPROM write-protect circuit. The board is also equipped with 48 internal general-purpose I/O bits and an external processor test port for loading and troubleshooting software.

1553 Board

The 1553 board is designed to operate as a remote terminal on a MIL-STD-1553B bus. The core component for the bus communication processing is the United Technologies Microelectronics Center SuMMIT chip, which communicates over the redundant bus under software control. Data are transferred to and from the RTX processor board through 32K words of shared memory, as well as internal registers in the SuMMIT chip, which are memory mapped on the expansion bus. The RTX

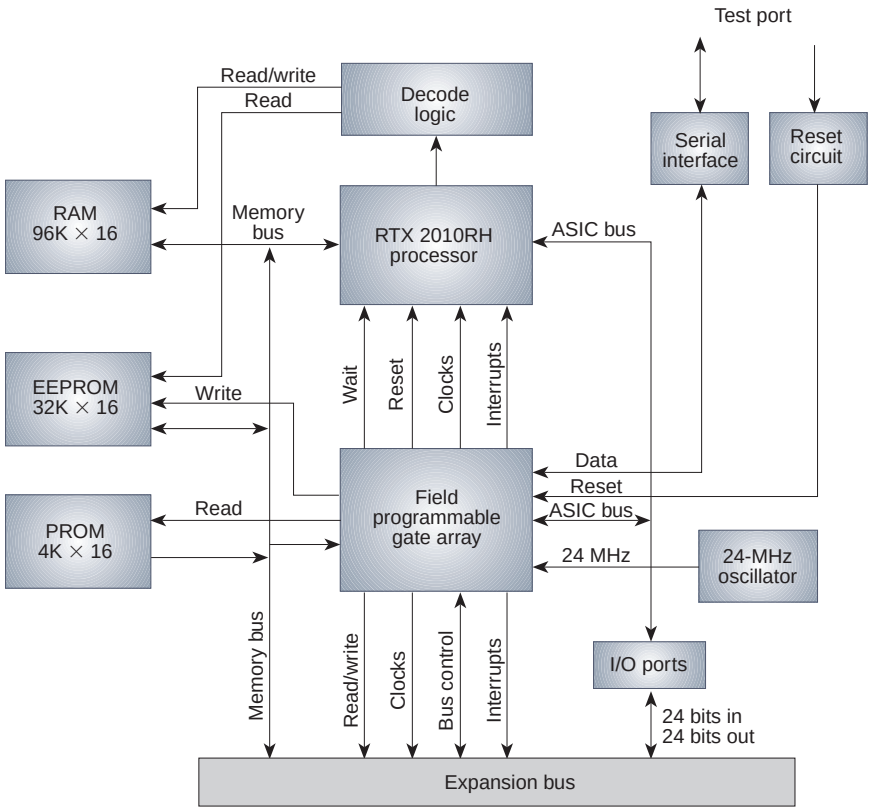

Figure 2. RTX processor board configuration. (ASIC = application-specific integrated circuit.)

processor board performs the arbitration for accessing the shared memory and shared registers. The board address, remote terminal address, and SuMMIT mode are configurable through the expansion bus connector.

In addition to the 1553 bus capabilities, this board has optically isolated inputs for spacecraft timing pulses from the NEAR command and telemetry processors. This signal is used to synchronize many of the DPU functions to a universal time.

Analog Input Board

The analog input board contains analog and digital electronics for gathering the instrument housekeeping and science telemetry data. This board is designed for four different input signal types: 5-V single-ended voltages, 5-V differential voltages, 50-mV differential voltages, and Analog Devices AD590 temperature sensors. The 50-mV differential voltage channels are for monitoring currents with an additional sense resistor. The board also has a flexible input configuration to allow some of the signals to be input from either the internal expansion bus connector or external connectors.

The 12-bit analog-to-digital converter and the input multiplexer are memory mapped and controlled by the processor through the expansion bus. The board address is configurable through the expansion bus connector.

Instrument Power Board

The instrument power board maintains ground isolation between the spacecraft power bus and the instruments and also adjusts the power of the bus, which can range from 22 to 34 V, to well-regulated levels, such as 5, 15, and –15 V. Although the power requirements of each instrument are different, the use of common components in their power boards maintained the modularity of the design. The common building blocks were defined and then combined to meet each instrument's requirements. A common backplane was also maintained for the power section of all the DPUs.

Each power board contains an inrush current limit circuit to prevent large surges when power is on, an Interpoint hybrid electromagnetic interference filter, up to four Interpoint hybrid DC-to-DC converters, and a low-voltage inhibit circuit that inhibits the converters if the spacecraft voltage drops below 18.5 V. In addition, some boards include a voltage regulator for outputs that require low current at voltages different from the available DC-to-DC converters. Current monitors compatible with the analog input board are implemented using a sense resistor in the input power return, and the AD590 sensors are used to monitor the temperature of the boards.

Some instruments require a means to command individual converters on and off. This feature was implemented using a solid-state relay in combination with the inhibit pin of the converters.

Power Motor Board

The power motor board performs three functions for the DPU. First, it conditions the power from the spacecraft to provide internal voltages at 5, 15, and –15 V using the common building blocks defined previously. Second, it provides the drive to instrument two-phase stepper motors. To minimize power dissipation on the power motor board, the current to each motor phase is regulated using pulse-width modulation. As part of the stepper motor control circuitry, interfaces for fiducial sensors monitor the motor position. Finally, this board can switch spacecraft power to another device, such as an operational heater, with its solid-state relay.

Instrument I/O Boards

In each instrument, the I/O board accommodates all unique instrument interfaces. The MSI I/O board is equipped with a 12-bit parallel input interface from the MSI for image data. This board also contains a 2-megabit serial link for high-speed image transfers to the solid-state recorder. The data to and from these interfaces are buffered using first-in-first-out memories. For real-time display of MSI images on ground support test equipment, the MSI I/O board has an image output test port.

The XGRS I/O board has an 8-bit parallel output and a 16-bit parallel input data bus to communicate with the XGRS. Eight discrete flags and six 24-bit counters are used to monitor sensor events. This board also provides a 12-bit parallel interface to control the high-voltage power supplies within the instrument.

The NIS/MAG I/O board controls and gathers data from both of these instruments. Discrete signals are used to control the NIS optics and analog-to-digital converters. Data from both NIS detectors are gathered via two parallel 12-bit interfaces and stored in 8K words of RAM on this board. This RAM is also used to store MAG data, which are gathered from the serial MAG data interface. The RAM is mapped onto the expansion bus and read out by the processor following an interrupt at the completion of the data gathering cycle. The configuration of the MAG is carried out through a serial command interface.

Instrument Memory Board

The instrument memory board provides for temporary internal storage of instrument data. Since the MSI is the only instrument requiring large amounts of internal storage, this board is unique to its DPU. Two copies of this board are installed to achieve a total of 2 MB of storage, mapped on the expansion bus in two

128K word pages. To access the entire 2 MB, memory pages are swapped by the RTX processor board through the general-purpose I/O bits. The board address is configured through the expansion bus connector.

PHYSICAL CHARACTERISTICS

Because of the common card size, all DPUs have the same footprint of 20.6 × 19.1 cm. However, the MSI DPU is taller than the rest to accommodate the extra memory boards. The dimensions of the MSI DPU are 20.6 × 19.1 × 19.8 cm, and the dimensions of the NIS/MAG and XGRS DPUs are 20.6 × 19.1 × 16.8 cm. The mass of the MSI DPU is 4.0 kg, the NIS/MAG DPU is 3.1 kg, and the XGRS DPU is 3.2 kg. Figure 3 is a photograph of the XGRS DPU.

Figure 3. The XGRS DPU.

CONCLUSIONS

By reusing common designs in multiple systems, the NEAR program saved significant resources in the development of the DPU hardware. In addition, the savings from the DPU hardware affected other areas of system development. For example, the common board size led to a common chassis design, reducing the mechanical engineering costs. The common processor allowed reuse of software routines, saving software development resources. Finally, the ground support test equipment shared many common components as a result of common interfaces in the DPUs. Thus, a modular design and reuse of components led to lower costs in many areas of development.

ACKNOWLEDGMENTS: The DPU development described in this article was performed at APL under a contract with NASA. The authors wish to acknowledge the contributions of John R. Hayes, Benjamin W. Ballard, Susan E. Schneider, S. Edward Hawkins, John O. Goldsten, Jeffery W. Warren, David A. Lohr, Albert A. Chacos, E. Brian Alvarez, Wolfger Schneider, E. Joseph Sheehi, and Jay J. Williams to the development of the NEAR DPUs. This work was supported under contract N00039-95-C-0002 with the U.S. Navy.

THE AUTHORS

CHRISTOPHER B. HERSMAN is a Spacecraft Systems Engineer in the Advanced Systems Group of Orbital Sciences Corporation. He received a B.S. degree in electrical engineering from the University of Cincinnati in 1988 and an M.S. degree in electrical engineering from the Ohio State University in 1990. Before joining Orbital in 1997, Mr. Hersman worked at APL for 7 years developing digital space-qualified electronic hardware for programs such as MSX and NEAR. While in school, Mr. Hersman also worked for Hughes Aircraft Company, Xerox Corporation, and Digital Equipment Corporation. His e-mail address is chris.hersman@orbital.com.

JOHN D. BOLDT is a member of the Space Sciences Instrumentation Group of APL's Space Department. He received a B.S.S.E. degree from South Dakota State University in 1982. Since joining APL in 1982, he has worked on spacecraft power systems and mission operations in addition to his current work with data systems for scientific instruments. He has designed data systems for the U1, U2, and U3 instruments on the Delta 180, 181, and 183 missions, the UVISI instruments on MSX, and the MIMI instruments flown on the Cassini mission to Saturn. Mr. Boldt was the lead engineer of the team that developed the common instrument data system design used by the NEAR instruments and the ACE ULEIS instrument. His e-mail address is john.boldt@jhuapl.edu.

PETER EISENREICH is a Senior Engineer in the Electronic Systems Group of APL's Space Department. He received a B.S.E.E. degree from Geneva College in 1982 and an M.S.E.E. degree from The Johns Hopkins University in 1987. Since joining APL in 1982, he has designed flight- and ground-based electronics systems on several projects, including AMPTE, GEOSAT, Polar BEAR, Delta 181, MSX, NEAR, AGRE, and FUSE. His specialty is the design of high-reliability, radiation-hardened flight electronics. Mr. Eisenreich designed the NEAR XGRS DPU and is currently the lead engineer of the FUSE instrument power-switching unit. His e-mail address is peter.eisenreich@jhuapl.edu.

STEPHEN F. ODEN received a B.S.E.E. degree from the Georgia Institute of Technology in 1962. After joining APL the same year, he assisted in the development of the AN/SRN-9 satellite navigation receiver prototype. He later worked on the Geoceiver satellite receiver, crystal oscillators for the SAS-A,B satellites, and the radar video preprocessor for the San Francisco Vessel Traffic System. In addition to his specialty in digital signal processing design, he was responsible for the digital filter bank subsystems for the SEASAT-A, GEOSAT, and TOPEX radar altimeters. He also assisted in the design of a synthetic aperture radar (SAR) data formatter for SEASAT-A, and was responsible for the design, fabrication, test, and integration of a SAR real-time wave spectra processor that flew on two shuttle missions in 1994. Mr. Oden recently completed the NIS/MAG DPU for NEAR and is currently developing the critical command decoder and the command and telemetry interface board for TIMED. His e-mail address is stephen.oden@jhuapl.edu.

DEANNA K. TEMKIN is a Principal Engineer from Orbital Science Corporation (OSC). In 1994, she began working in APL's Space Department as a resident subcontractor. She received a B.S. degree in electrical engineering from the University of Virginia in 1983 and an M.S.E.E. degree in microelectronics from the University of Maryland in 1987. Since joining OSC in 1984, her primary tasks have included designing and developing power electronics space-qualified hardware, including DC-to-DC converters, power system electronics, motor controllers, and current amplifiers. She has flight hardware on TOPEX, SMEX, TRMM, XTE, EOS, NEAR, and ACE satellites. Ms. Temkin is currently a lead engineer for the TIMED IEM power converter boards and power-switching and distribution unit. Her e-mail address is deanna.temkin@jhuapl.edu.