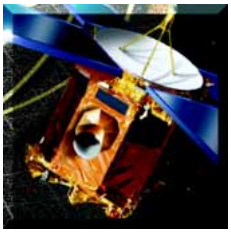

The NEAR Solid-State Data Recorders

Ronald K. Burek

Data recorders make it possible for the Near Earth Asteroid Rendezvous (NEAR) spacecraft to delay and slow the transmission of information to Earth, thereby accommodating the temporal and bandwidth limitations of the communications link. NEAR is the first spacecraft developed by the Applied Physics Laboratory to employ solid-state recorders, supplanting magnetic tape recorders used previously. Also, the 132 dynamic random-access memory devices, which are at the heart of the NEAR recorders, constitute the first large-scale use of plastic encapsulated microcircuits on a Laboratory spacecraft. Earlier spacecraft relied almost exclusively on hermetically packaged microcircuits. Several measures, including two layers of error detection and correction, were taken to mitigate the effects of single-event upsets that may be induced by charged particles in space.
(Keywords: Memory, Plastic, Recorder, Spacecraft, Storage.)

INTRODUCTION

The Near Earth Asteroid Rendezvous (NEAR) spacecraft is the first APL spacecraft to use solid-state data recorders (SSDRs) for mass storage. It is also the first APL spacecraft to use plastic encapsulated microcircuits (PEMs) in significant numbers. Prior to NEAR, APL had launched 18 magnetic tape recorders on nine spacecraft. These tape recorders ranged in storage capacity from 5 megabits (Mb) to 54 gigabits (Gb). Earlier still, the Transit series of APL spacecraft used arrays of magnetic cores with as much as 32 kilobytes of capacity. By comparison, the two NEAR recorders together can store 1.6 Gb of user data in 132 PEMs. Each PEM is a 16-Mb dynamic random access memory (DRAM) integrated circuit. The performance parameters and spacecraft accommodation requirements for the NEAR SSDRs are summarized in Table 1.

When radiation-tolerant semiconductor memories reached a density of 256 kilobits per integrated circuit, they began to seriously challenge the use of magnetic tape in space. With the availability of 16-Mb devices, such as those used in the NEAR SSDRs, the 35-year reign of tape recorders is nearly ended. Three tape recorders for Japan and one for Canada are probably the last ones being manufactured to operate aboard unmanned spacecraft.

SSDRs have many advantages over tape recorders. They are smaller, lighter, and less expensive. They also use less power and impart no momentum or vibration disturbances to the spacecraft. The inherent

Table 1. Characteristics of the NEAR solid-state data recorders (SSDRs).

Characteristic	SSDR 1	SSDR 2
User storage capacity	2^{30} bits ≈ 134 megabytes	2^{29} bits ≈ 67 megabytes
Input/output data rates	Record: 0 to 2,002 kilobits/s	Record: 0 to 2,002 kilobits/s
(nonsimultaneous)	Playback: 0 to 400 kilobits/s	Playback: 0 to 400 kilobits/s
Input/output format	Serial NRZ-L	Serial NRZ-L
Storage media	(88)[a] 4 megabits × 4 IBM Luna-C DRAMs	(44)[a] 4 megabits × 4 IBM Luna-C DRAMs
Telemetry	540 bytes, serial NRZ-L	540 bytes, serial NRZ-L
Commands	48 commands, serial NRZ-L	48 commands, serial NRZ-L
Nominal power requirements	6.8 W at 28 V DC	5.2 W at 28 V DC
Mass	1.64 kg, excluding harness	1.34 kg, excluding harness
Envelope	Footprint: 17.9 × 12.1 cm; height: 8.2 cm	Footprint: 17.9 × 12.1 cm; height: 8.2 cm

[a]Refers to the total number of dynamic random access memory (DRAMs) devices.

redundancy and reconfigurability of their memory arrays and an overall lower parts count improve reliability. They also tolerate a much wider range of operating temperature than magnetic tape. Perhaps their biggest advantage is operational flexibility, since they are randomly addressable and can easily accommodate discontinuous data at widely varying rates. These advantages outweigh the volatility of current SSDRs—if power is lost, all data are lost. This shortcoming is an acceptable trade-off for NEAR.

The NEAR spacecraft uses the SSDRs to store science and engineering data temporarily during those periods when effective communication with the Earth is not possible or is constrained by bandwidth. In the former case, the stored data are played back at scheduled times when communication is possible. In either case, an SSDR can play back the data at a fraction of the record rate to accommodate the communications link.

Commonality and Heritage

The Discovery concept emphasizes the use of off-the-shelf hardware, proven designs, and low cost. In keeping with this notion, SEAKR Engineering, Inc., provided the SSDRs for both NEAR and the Advanced Composition Explorer (ACE) spacecraft, which were built at about the same time. To reduce costs, the two spacecraft programs agreed to use virtually identical specifications. Slight differences, mostly in environmental and performance assurance requirements, were generally enveloped. The architecture and firmware of the SSDRs were largely those of Clementine-1, which evolved from six earlier SSDRs.

The changes to the Clementine design involved mostly hardware and parts selection. Clementine used 4-Mb DRAMs packaged in multichip modules. The substitution of 16-Mb discrete PEM DRAMs resulted in significant savings in power, mass, size, cost, and time. For NEAR and ACE, these advantages far outweighed the disadvantages of having to redesign the memory modules and to accommodate the 3.6-V DC operating voltage and unusual upset modes of the 16-Mb DRAMs.

Other changes, such as from parallel input/output (I/O) to serial I/O, and from single to multiple formats for the telemetry, were relatively minor by comparison. So too was the substitution of a different DC/DC converter and the addition of circuitry to limit the inrush of current at power turn-on. The ACE SSDRs gave up the initial requirement for simultaneous read and write, but gained from lessons learned during the development of the NEAR SSDRs. The NEAR SSDRs benefited in terms of schedule and gained much of the radiation tolerance enveloped around the ACE SSDRs. The commonalities and heritage significantly lowered costs for both programs.

Dynamic Random-Access Memory

Commercial DRAM devices used in personal computers are the de facto enabling technology for SSDRs. However, they must also be able to operate in the space radiation environment of a given mission. The IBM Luna-C 16-Mb DRAM was found to have unusual tolerance to the harsh radiation environment of the ACE mission. It is free from latchup in a charged-particle environment and can survive a moderately high total dose. Most importantly, its single-event upset (SEU) modes proved to be amenable to relatively simple mitigative measures.

DESIGN OVERVIEW

The fundamental design approach for the SSDRs is fairly uncomplicated. Incoming data are captured from one of two serial data lines, latched into static random access memory (SRAM) buffers, and encoded by an error detection and correction (EDAC) system. The encoded data are transferred to the DRAM memory array via an internal bus. Playback is performed by reading the words out of the array and correcting all single-bit errors and some double-bit errors. The bus data are converted to serial form and then shifted out to the command and data handling subsystem.

As shown in Fig. 1, the SSDR electrical interfaces with the spacecraft consist of data I/O, command, telemetry, and +28 V DC power connections. The electronics are partitioned into memory, power, and control modules, with an interconnecting motherboard. The assembly is housed in an aluminum enclosure. Figure 2 is a photograph of a NEAR SSDR prior to conformal coating.

Memory Modules

One of the NEAR SSDRs contains two memory modules, and the other contains one. Each module consists of two printed wiring boards, each with 22 DRAMs, mounted back-to-back and epoxy-bonded to an aluminum plate. The boards also include voltage-level translators that adapt the 3.6-V DRAMs to the 5-V logic of the controller.

Power Module

The power module consists of a single board. Besides the power conditioning circuitry and power connector, it also contains the data I/O, command, and telemetry interface circuitry and connector. The power conditioning circuitry employs an inrush current limiting circuit as well as electromagnetic interference filter and DC/DC converter modules. The 28 V from the spacecraft is converted to 5 V for use by most of the SSDR circuitry. A linear regulator provides 3.6 V for the DRAMs.

Controller Module

The controller consists of two boards, mounted back-to-back like the memory modules. Overall control and data flow orchestration are performed by an imbedded 80C85 microprocessor. A radiation-hardened version from Harris Semiconductor is used, which is single-event latchup (SEL) and SEU immune.

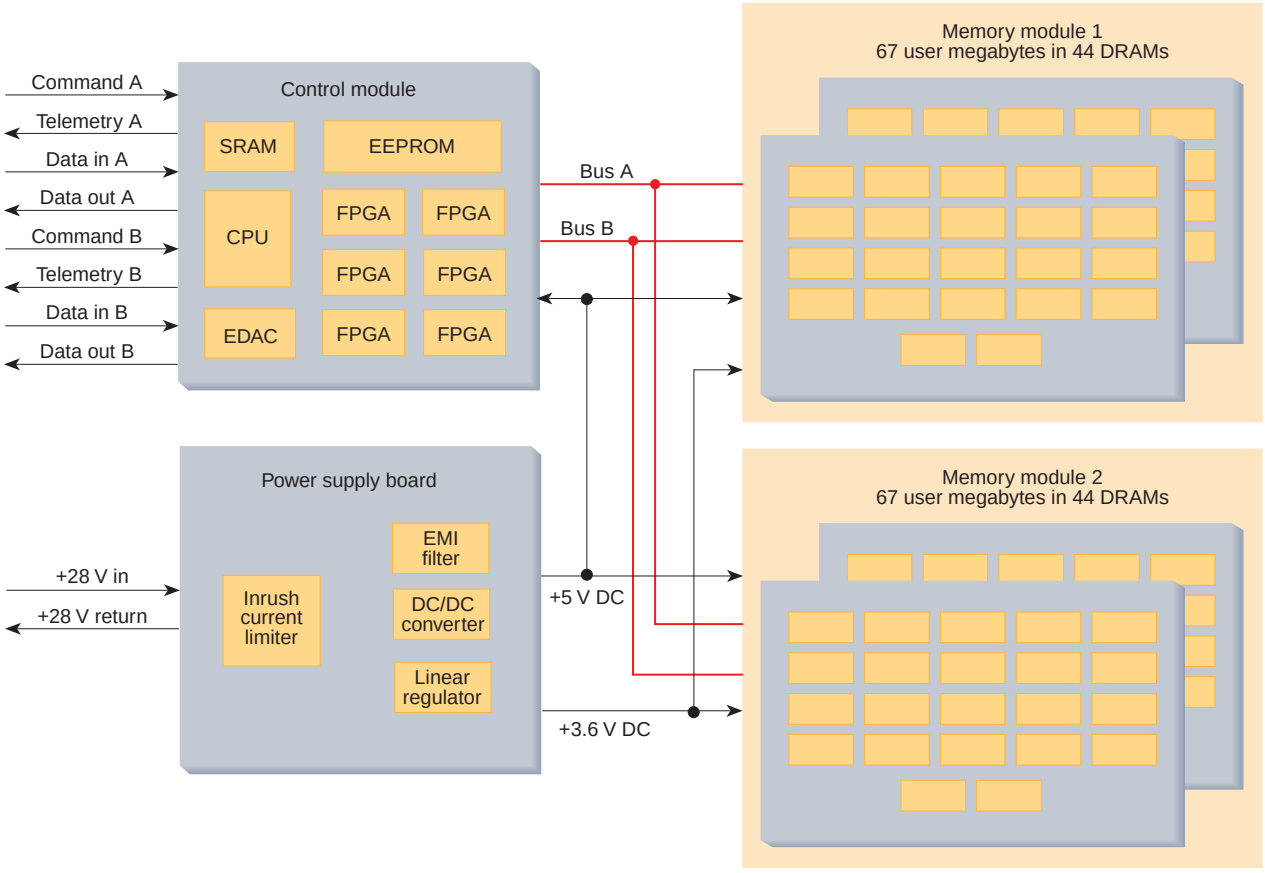

Figure 1. System-level block diagram of the NEAR solid-state data recorders. Note: NEAR has only one memory module in one unit. (SRAM = static random-access memory, EEPROM = electrically erasable programmable read-only memory, CPU = central processing unit, FPGA = field programmable gate array, EDAC = error detection and correction, EMI = electromagnetic interference, DRAM = dynamic random access memory.)

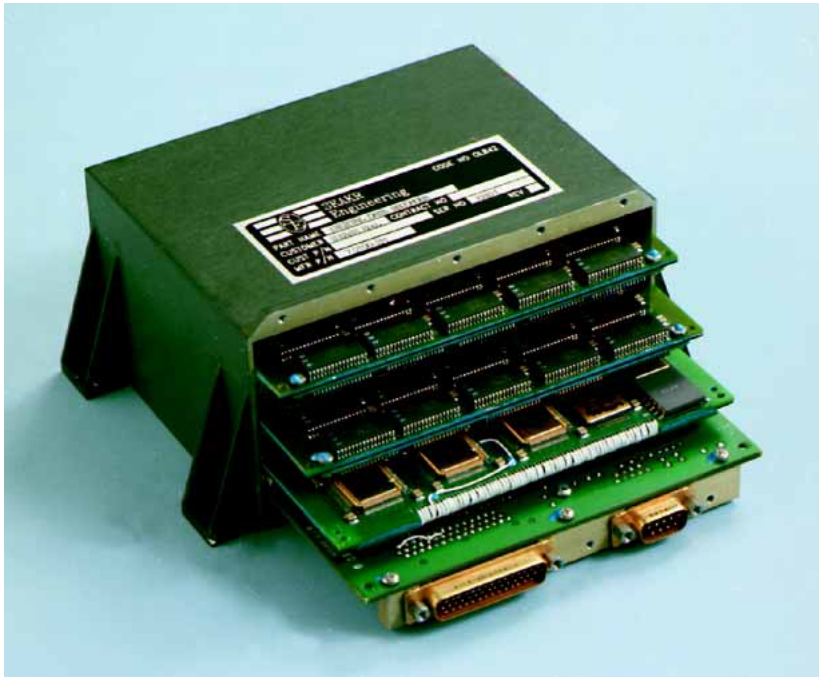

Figure 2. NEAR solid-state data recorder prior to conformal coating. Footprint: 17.9 × 12.1 cm; height: 8.2 cm.

A SRAM array serves as a scratch pad for the microprocessor. The SRAM is SEL free and SEU tolerant. It also facilitates in-flight reprogramming by means of the serial command port of the SSDR. An electrically erasable programmable read-only memory (EEPROM) stores the bootcode and firmware for the microprocessor. The EEPROM is SEL/SEU free.

A radiation-hardened chip implements a modified Hamming code to perform external EDAC during scrubbing and user data I/O operations. Several field programmable gate arrays are used to perform DRAM scrub and refresh, control, formatting, and direct memory functions. To mitigate errors from SEUs in the field programmable gate arrays, all critical registers are triplicated and use majority voting. In addition, critical registers are periodically refreshed. The bootcode and firmware for the microprocessor are written in a combination of C and 80C85 assembly language. The firmware employs a number of strategies to facilitate autonomous recovery from upsets.

Plastic Encapsulated Microcircuits

The use of PEMs for spaceflight and military applications has traditionally been forbidden. Relative to hermetically packaged microcircuits (HPMs), PEMs have long been perceived as a reliability risk. Meanwhile, the market for PEMs in commercial and consumer electronics has grown to dwarf that of HPMs for aerospace. As a result, the sources of HPMs are rapidly disappearing. Increasingly, the latest and most desirable integrated circuits, such as the DRAMs used in the SSDRs, are available only as PEMs. All the while, the reliability of PEMs has been steadily improving. Accordingly, the APL Space Department studied the feasibility of safely using them in space. The study [1,2] concluded that properly qualified and applied PEMs could indeed be used for spaceflight. The study described and recommended storage, design, and fabrication practices that were particularly applicable to PEMs. Chief among these were measures intended to prevent the ingress of moisture. These measures included, for example, storage in low-humidity conditions and bakeout prior to conformal coating. The study also outlined a regimen for qualification, screening, and quality conformance inspection that was equivalent to MIL-STD-883 standards. To the extent possible, the IBM Luna-C 16-Mb DRAMs were implemented in the SSDRs in accordance with the recommendations of the study.

Single-Event Upset Mitigation

Charged particles may cause SEUs in the SSDR by flipping bits in the controller circuitry or within the DRAMs that constitute the memory array. The aforementioned use of radiation-hardened or radiation-tolerant parts, triplication and majority voting, watchdog timer, and firmware countermeasures prevent or mitigate the occurrence of SEUs in the controller. However, the DRAMs constitute by far the bulk of the semiconductor volume susceptible to SEUs. In fact, the IBM Luna-C DRAMs were found to have three upset modes: functional interrupts, single data-bit upsets, and redundancy latch upsets. These required three kinds of countermeasures.

The functional interrupt is the least important upset. It causes a DRAM to switch into an internal test mode, which prevents normal use. The only way to recover is to power cycle the DRAM or map around it. The latter step reduces the storage capacity of the SSDR. Either step results in lost data. Fortunately, the upset rate for this event is calculated to be acceptably low, even during worst-case solar flares. Thus, either power cycling the entire SSDR or mapping out the DRAM is an acceptable countermeasure.

Single data-bit upsets cause errors within the DRAM memory array itself. The upset rate for this event is low enough to be able to rely upon the EDAC system internal to each Luna-C DRAM.

The effects of a redundancy latch upset are much more severe as measured by the upset rate and number of bits affected per upset. To increase manufacturing yield, the Luna-C has several extra rows and columns. During wafer and die tests, they are used to replace defective rows and columns. This replacement is effected via laser trimming to bias the inputs of a bistable redundancy latch. An upset of one of these latches causes the loss of up to 1024 pairs of data bits. Because of the architecture of the DRAM, such a loss always manifests itself as errors in data bits 0 and 1 or in data bits 2 and 3 of a given DRAM. To counter this kind of error, the SSDR uses an external EDAC system that can scrub the memory array of this particular kind of paired error.

Scrubbing

Memory scrubbing consists of reading the contents of each memory location, correcting the data by using the external EDAC system, and writing the corrected data back into the location from which it originated. Since random bits are upset in the DRAMs at random times, it is necessary to periodically scrub all of the data in the memory array. The frequency of this scrubbing is referred to as the scrub rate. The required scrub rate is dictated by the rate at which SEUs occur within the memory array and by the error correction capability of a given EDAC system. The rate of SEUs is derived, for a given space radiation environment, from empirical data for each given type of integrated circuit. Several commandable scrub rates, which bracket the required rate, are provided in the NEAR SSDR.

Memory Reconfiguration

The controller monitors the health of the DRAM array based on the scrub operations. The descriptions and the locations in the array of any uncorrectable errors found during scrubbing can be stored in tables. In addition, a list of locations in the array currently in service is maintained in another table. Any of the tables can be telemetered. By command, the user has the option of partially or completely changing the latter table based on information contained in the former tables. In this way, the DRAM memory can be logically reconfigured into a contiguous error-free array at any time, regardless of uncorrectable bit errors, should any occur.

Error Detection and Correction

The SSDRs incorporate two layers of EDAC, internal and external to the DRAMs. Internal to each DRAM is a built-in EDAC system that uses a 137-bit Hamming code to correct errors originating in the memory array. Each DRAM is internally divided into four quadrants, each of which stores data as a 128-bit word, and each word is protected by nine check bits. Each time data are read, a syndrome is computed. If a single bit error is present, it is corrected; if a double bit error occurs, it is flagged.

The external EDAC system twice uses a modified Hamming code. Check bits are appended to the data to create a code word capable of correcting a single bit error. Two of these code words are combined in such a way that all even bits occur in the first code word and all odd bits occur in the second code word. In this way, any single erroneous bit or any single odd–even pair of erroneous bits can be corrected. This setup allows the external EDAC system to overcome a redundancy latch upset.

OPERATION

A menu of 48 commands, together with more than 540 bytes of status and health telemetry, provides a great deal of flexibility and information to the user in conducting flight operations with the SSDRs.

Commands

The SSDRs have four basic operation modes: idle, record, playback, and built-in test. The SSDR may sequence between these modes upon command. Command data consist of one or more 16-bit words. Each command contains an opcode, 0 to 127 fields, and usually a checksum. The DRAM memory may be partitioned into eight or fewer segments. Each segment is dynamically allocated as defined by command and data clocks. Segments may be sequentially or randomly accessed via 16 record segment or random record commands, or via 16 playback segment or random playback commands. Other commands are available to change DRAM refresh or scrub rates, perform built-in test or reset, reprogram the microprocessor, change telemetry and data ports, or reconfigure the DRAM array so as to sidestep uncorrectable errors should any occur.

Telemetry

Default telemetry describes the up-to-the-second status of the SSDR. These bits indicate mode, read and write pointer locations, segment and memory configuration, command validity and history, scrub and refresh rates, and built-in test results. Additional telemetry is available to the user upon command, which thoroughly reports on any errors corrected or detected by the external EDAC system. The reported errors are distinct from any errors corrected internally by the DRAMs themselves whenever their data are read out. Internal corrections are not reported. As with most spacecraft subsystems, the internal temperature, DC/DC converter voltage, and current for each SSDR are also telemetered.

SUMMARY

The two NEAR data recorders can together store up to 200 megabytes for later playback to Earth at reduced data rates. The storage elements are 132 DRAMs, supplanting the magnetic tape heretofore used for mass storage on most spacecraft. The DRAMs represent the first large-scale use of PEMs in APL spacecraft. In preparation for the encounter with the asteroid Mathilde, the smaller of the two recorders was turned off on 18 April 1997. It had operated flawlessly since before launch; no errors had been reported by its external EDAC system. Now that the spacecraft was closer to the Sun, the larger recorder assumed the primary role, and the smaller unit acted as a spare.

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