The MSX Tracking, Attitude, and UVISI Processors

Laurence J. Frank, Christopher B. Hersman, Stephen P. Williams, and Richard F. Conde

The Applied Physics Laboratory has developed a general-purpose spacecraft computer suitable for many subsystem applications on the Midcourse Space Experiment (MSX) spacecraft. This article presents the major features of the computer and common interface boards and describes three MSX subsystems that use them.

COMPUTER REQUIREMENTS AND DESIGN TRADE-OFFS

The amount of electronics involved in the Midcourse Space Experiment (MSX) required that common designs be used wherever possible. Three instruments—the tracking processor, the attitude processor, and the Ultraviolet and Visible Imagers and Spectrographic Imagers (UVISI) image processor—each use a general-purpose computer designed for MSX as well as common interface boards.

Reference 1 describes the system requirements, design trade-offs, and computer features in great detail. Those features are summarized in what follows (see also Table 1).

Computer Features

The single-board computer implements an expanded-mode MIL-STD-1750A computer. The core of the computer is a silicon-on-sapphire version of Performance Semiconductor's 1750A chip set. This chip set provides the required computational throughput and is supported by commercially available development tools and compilers. The silicon-on-sapphire version of the chip set was chosen because of its superior radiation characteristics. It consists of three integrated circuits: the central processing unit (CPU, P1750A), the memory management unit/combination (MMU/Combo, P1753), and the processor interface circuit (P1754). In the MSX design, the chip set operates at up to 20 MHz with two wait states, providing an estimated 1 million instructions per second of processing capability using a Digital Avionics Instruction Set mix. Other features on the board include 256K words of static random access memory (RAM), 2K words of programmable read-only memory (PROM), an interface to a simple bus for connection to peripherals, a memory expansion bus, and an emulation and test port.

The Performance chip set contains several "built-in" features that otherwise would have been implemented in external hardware. One such feature is error detection and correction (EDAC), which is done by the MMU/Combo chip. With EDAC checking enabled, this chip can correct single bit errors and detect double

Table 1. Processor design features and specifications.

Feature	Specification
Software environment	
Processor	Expanded-mode MIL-STD-1750A
Throughput	1 million instructions/s Defense Avionics Instruction Set mix
Development tools	Tektronix 8540A development system
	Tektronix DAS-9200 logic analyzer
	PC-based console device
Language support	Various Ada compilers (Tartan used for MSX)
Boot PROM (programmable read-only memory)	2K words
RAM (random access memory)	256K words of EDAC SRAM (error detection and correction static RAM) on processor board and optional memory board
EEPROM (electrically erasable PROM)	256K words on optional memory board
PROM	32K words on optional PROM board
Radiation characteristics	
Total dose radiation tolerance	>15 krad (Si)
Single-event upset rates for typical low-Earth orbit	Processor: $<5.5 \times 10^{-5}$ errors/day
	RAM: $<1.1 \times 10^{-8}$ errors/day (with EDAC)
	EEPROM: $<4.2 \times 10^{-9}$ errors/day
Electrical design	
Supply voltage	4.5–5.5 V
Power consumption (for two-board set)	5 W (worst case), 3 W (typical)
Emulation and test interface	Tektronix 8540A (transistor-transistor logic–compatible complementary metal oxide semiconductor [CMOS])
Back-plane interface	Custom bus (simple address, control, and data)
Electronics	All advanced CMOS (logic families)
Mechanical design	
Board size	18 × 30 cm
Connectors	Back plane: 180-pin (from AMP,inc.) (1)
	Emulation and test: 50-pin, D type (2)
	Serial interface: 9-pin, D type (1)
Board weight	<0.68 kg
Thermal design	
Temperature range (chassis)	240 to 1660°C

bit errors. The presence of EDAC allows the use of commercial RAM chips that are denser but less radiation-tolerant than the largest available flight-qualified RAM chips.

The socketed PROM provides permanent, nonvolatile storage for start-up code. The system bus is located on a back-plane connector, which furnishes a simple method to connect custom hardware to the processor. The memory expansion bus allows for a high-speed connection to additional RAM on a different board. Eight user interrupts are available on the system bus connector. The emulation and test port allows card-edge emulation, logic analysis, and an interface to a PC-based console debugger.

EEPROM/RAM Expansion Board

All applications described in this article necessitate more RAM than that available on the processor board and also require nonvolatile, writable memory to store application code. These needs resulted in the development of the electrically erasable PROM (EEPROM)/RAM expansion board.

The EEPROM/RAM board affords an additional 256K words of EDAC RAM, which connects to the processor via the memory expansion bus. It also provides 256K words of nonvolatile storage in EEPROM (which connects to the processor via the system bus) and expands the number of system interrupts from 8 to 22 through the use of two standard interrupt controllers. A single RS-422 serial line interface is available on an external connector.

COMMON INTERFACE BOARDS

The use of a common computer setup allowed the design of common interface boards. The attitude processor, tracking processor, and UVISI image processor all have identical interfaces to the spacecraft's command processors and data handling system (DHS). In addition, they all require hardware features not implemented on the 1750A unit or EEPROM/RAM boards such as additional boot PROM, a timing chain, and interfaces to

other processors. Two common interfaces were therefore developed for use in all three processors.

The first of these two boards, the spacecraft input/output (I/O) No. 1 board, implements two interfaces to the redundant command processors and three interfaces to the redundant DHS. The interfaces to the command processors include a 32-bit serial command interface and a memory load interface that can handle serial data loads as long as 2048 bits. The three serial interfaces to the DHS include one used to transfer housekeeping telemetry to the DHS, one to transfer memory dump data to the DHS, and one to receive Universal Time (UT) from the DHS. A radiation- hardened 80C85 microprocessor serves as an interface controller for the 32-bit serial command interface and UT interface. The use of the microprocessor as an interface controller offers several benefits: it reduces the overall number of parts required to implement the interfaces, provides fault protection for the interfaces, and unloads the 1750A processor from management of the interfaces. The 80C85 is programmed in assembly language, with code residing in a 2K × 8 PROM.

A second common interface board, the spacecraft I/O No. 2 board, contains two more interfaces to the DHS, an additional interface to the command processors, a bidirectional serial interface to another processor, up to 4K × 8 of additional boot PROM, and a timing chain. One of the interfaces to the DHS is used to transfer science data. The additional command interface allows 64-bit commands to be sent to the command processors.

A standard serial interface was defined to reduce the number of interface types. It consists of three signals—enable, clock, and data—all generated by the subsystem sending the message, and is used widely by the attitude, tracking, and UVISI processors. A gate array, known as the controller, has been developed to control this interface. It contains circuitry to read 8 or 16 bits of parallel data from standard 512 × 8 first-in/first-out devices (FIFOs), to generate the three signals that make up the interface, to receive data from the standard interface, and to write 8 or 16 bits of parallel data to FIFOs. The controller allows the use of redundant inputs and outputs, with a maximum input/output serial data rate of 1.25 Mbits/s. It is fabricated on a United Technologies Microelectronics Center radiation-hardened complementary metal oxide semiconductor (CMOS) gate array.

The controller is used on spacecraft I/O boards 1 and 2. Both the attitude and tracking processors have additional interfaces that are implemented using the standard serial interface. This configuration led to the development of a third common interface board, serial I/O board No. 1, which is used only on the attitude and tracking processors and contains hardware to support up to five standard serial interfaces. Figure 1 is a block diagram of the tracking processor and shows how the common boards interface to other subsystems.

Three types of miscellaneous logic are used for the common interface boards: advanced CMOS logic for the system address and data buses, decoding logic, and high-speed clocks; high-speed CMOS (HCTS) parts where medium-speed logic is required; and CD4000 logic for low-speed (16 kHz or less) interfaces. RS-422 line drivers and receivers, the 26LS31 and 26LS32, respectively, are used on the standard serial interfaces.

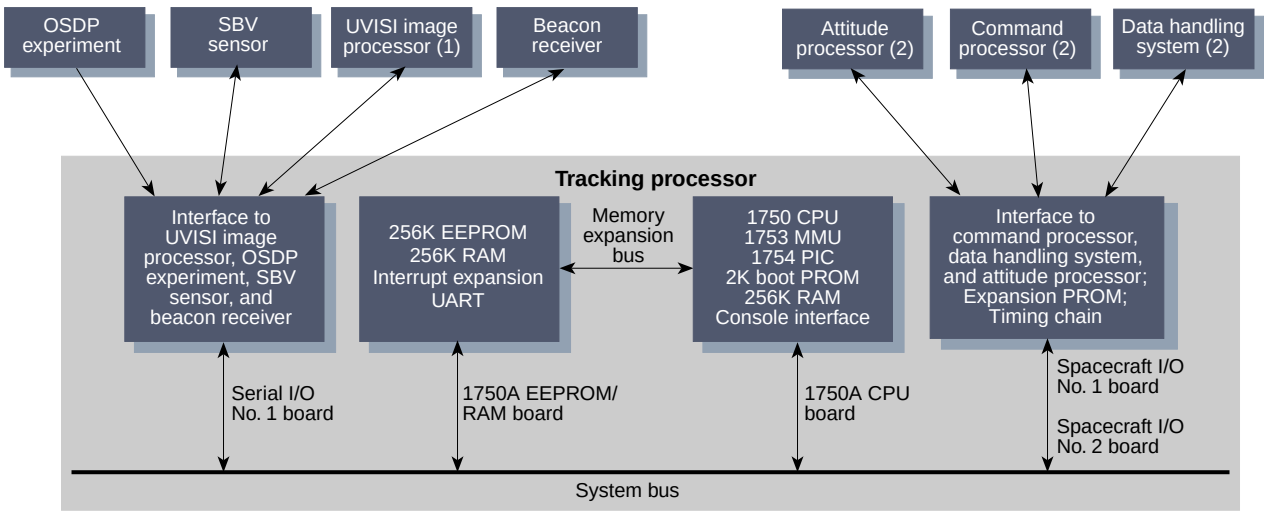

Figure 1. Block diagram of the tracking processor and interfaces. (OSDP = Onboard Signal and Data Processor, SBV = Space-Based Visible, PROM = programmable read-only memory, UVISI = Ultraviolet and Visible Imagers and Spectrographic Imagers, EEPROM = electrically erasable PROM, RAM = random access memory, UART = universal asynchronous receiver/transmitter, CPU = central processing unit, MMU = memory management unit, PIC = processor interface unit, I/O = input/output.)

APPLICATIONS

Attitude Processor

The attitude processor (see Ref. 2 for a detailed description of its hardware and software) is a redundant subsystem that uses data inputs from a number of attitude sensors as well as time and ephemeris data to control MSX attitude. This application demands both high reliability and a significant processing capability. Pointing and maneuvering functions are critical to mission success and spacecraft safety. The high throughput capability is required to execute the complex algorithms that control vehicle orientation and stability.

Each redundant attitude processor includes two 1750A CPU boards and two EEPROM/RAM expansion boards. One pair of boards is used as an I/O processor to handle the high data throughput needed to monitor the spacecraft attitude sensors and actuate control elements. The other pair executes the attitude control program that provides the closed-loop spacecraft pointing and maneuvering control required by the MSX. The two 1750As that comprise the attitude processor are loosely coupled. They operate on independent buses, control different interface boards, and communicate via standard serial interface. The attitude subsystem software is loaded from EEPROM to RAM upon initialization and then executed from RAM to increase speed. Internal interface boards allow data to be passed between the pair of processors in the attitude control subsystem. The attitude control programs can be modified and reloaded after launch.

In addition to the three common interface boards already described, the attitude processor contains three unique interface boards that have additional interfaces to attitude subsystem components: a special test port and the interface between the two 1750A processors. Attitude subsystem and other components that interface to the attitude processor include a star camera, Sun sensors, Earth sensors, gyros, reaction wheels, torque rods, a magnetometer, solar panels, and antenna gimbals. Each attitude processor also has interfaces to both tracking processors.

Each redundant attitude processor contains ten 18 × 30 cm multilayered printed circuit boards, a multilayered motherboard, a power filter board, and internal wiring. Each weighs 12.45 kg and dissipates 13 W of secondary power.

Tracking Processor

The tracking processor interprets data from multiple MSX science instruments and spacecraft subsystems in order to identify objects in the field of view of the spacecraft's sensors, including the UVISI image processor, the beacon receiver, the Space-Based Visible sensor, and the Onboard Signal and Data Processor (OSDP) experiment. It performs computationally intensive tracking tasks. In addition, it analyzes sensor data to identify test objects using knowledge about the motion of the spacecraft, anticipated background viewing conditions, and known sensor characteristics.

Redundant tracking processors make up the tracking subsystem; only one is operated at any given time. Each includes a 1750A CPU board, an EEPROM/RAM expansion board, and the three common interface boards described previously. As with the attitude processor, the application software is loaded into RAM from EEPROM after system initialization, and software can be modified and reloaded after launch.

Each redundant tracking processor contains five 18 × 30 cm multilayered printed circuit boards, a multilayered motherboard, a power filter board, and internal wiring. Each unit weighs 7.25 kg and dissipates 6 W of secondary power.

UVISI Image Processor

The UVISI image processor is responsible for analyzing UVISI sensor images to locate, identify, and characterize objects in the field of view. It serves as one of the data sources for the tracking processor described earlier. Initial image processing is done in dedicated hardware, followed by processing in a general-purpose digital signal processor; the remaining processing is performed in a 1750A processor. The image processing algorithms are in software and can be uploaded. This processor is a nonredundant subsystem composed of six circuit boards. The attitude and tracking processors have four boards in common: the 1750A processor board, the EEPROM/RAM expansion board, and both spacecraft I/O boards. The 1750A CPU board controls the overall subsystem operation and performs limited image processing. The EEPROM/RAM expansion board enables the image processing code to be reloaded after launch. The spacecraft I/O No. 1 board provides interfaces to the command processors and DHS. The spacecraft I/O No. 2 board contains additional PROM storage for 1750A boot code and a bidirectional interface to each tracking processor.

The image processor contains two unique boards, the preprocessor board and the digital signal processor (DSP) board. The preprocessor board has interfaces to each of the redundant UVISI data control systems (DCS). These interfaces allow the image processor to request images from one of the four UVISI cameras, receive images from the selected UVISI cameras, receive information about the image being transferred, and output status information to the DCS. The image preprocessing section of the board contains a windowing function that allows selection of areas of interest in a UVISI camera image for further processing. The size

and location of the window are controlled by software running on the 1750A processor. The contents of the window can be compressed in hardware, allowing a wider field of view with less resolution. The contents are sent to the DSP board, which employs an Analog Devices ADSP-2100 DSP and contains 364 KB of RAM for holding code, coefficients, and images. The 1750A has direct access to most of this memory for downloading code and coefficients to it from the EEPROM/RAM expansion board. The DSP board software performs all of the low-level image processing and provides a thresholded (binary) image to the 1750A for further processing.

The UVISI image processor contains six 18 × 30 cm multilayered printed circuit boards, a multilayered motherboard, a power filter board, and internal wiring. Each unit weighs 7.7 kg and dissipates 6 W of secondary power.

REFERENCES

[1] Frank, L. J., Hersman, C. B., Williams, S. P., and Conde, R. F., *A General-Purpose MIL-STD-1750A Spacecraft Computer System*, AIAA 93-4465, AIAA Computing in Aerospace 9 Conference (1993).

[2] Williams, S. P., Kennedy, L., Frank, L. J., and Pham, R., *A Low Power, Radiation Tolerant Spacecraft Attitude Processor*, AIAA 93-4492, AIAA Computing in Aerospace 9 Conference (1993).

ACKNOWLEDGMENT: The MSX mission is sponsored by the Ballistic Missile Defense Organization. This work was performed under contract N00039-94-C-0001.

THE AUTHORS

LAURENCE J. FRANK received his B.S.E.E. degree from Catholic University of America, Washington, DC, in 1978. From 1977 through 1982 he worked for the Naval Research Laboratory in Washington, DC, designing instrumentation for underwater acoustics research. He joined APL in 1982 and has worked in the Spacecraft Flight Systems Group ever since. Mr. Frank has designed hardware and software for spacecraft subsystem avionics ground systems and ground support equipment. He has been the systems engineer for a number of instruments and space mission development efforts. His e-mail address is Laurence.Frank@jhuapl.edu.

CHRISTOPHER B. HERSMAN received his B.S.E.E. degree from the University of Cincinnati in 1988. During his cooperative education, he worked for Hughes Aircraft Company, Xerox Corporation, and Digital Equipment Corporation. After receiving his M.S.E.E. degree from the Ohio State University, he joined APL in 1990. Mr. Hersman has worked on numerous MSX program subsystems. Initially, he wrote software for the UVISI instrument ground support equipment software. Later, he took part in the development of the data handling system flight hardware. Mr. Hersman is now lead engineer for the Near-Earth Asteroid Rendezvous multispectral imager data processing unit. His e-mail address is Christopher.Hersman@jhuapl.edu.

STEPHEN P. WILLIAMS graduated from Duke University with a B.S. in biomedical engineering in 1975 and was awarded an M.S. in electrical engineering from North Carolina State University in 1980. He joined APL in 1980, and has been in the Space Department's Spacecraft Flight Systems Group since then. Mr. Williams has designed flight hardware or software for numerous APL spacecraft, including Polar BEAR, Delta 180, Delta 181, the Active Magnetospheric Particle Tracer Explorers, MSX, and the Advanced Composition Explorer. His e-mail address is Stephen.Williams@jhuapl.edu.

RICHARD F. CONDE received a B.S. in electrical engineering from Cornell University in 1981 and an M.S. in electrical engineering from The Johns Hopkins University G. W. C. Whiting School of Engineering in 1985. He joined APL in 1981 and is a senior staff member of the Spacecraft Flight Systems Group. Mr. Conde has worked on a variety of flight systems on the Geosat, Polar BEAR, Delta 180, Delta 181, and MSX spacecraft. He is currently lead engineer for the Advanced Composition Explorer spacecraft command and data handling subsystem. His e-mail address is Richard.Conde@jhuapl.edu.