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A SPACE-BASED HIGH-SPEED DIRECT DIGITAL SYNTHESIZER MULTICHIP MODULE USING LOW-TEMPERATURE CO-FIRED CERAMIC

The Mid-Course Space Experiment S-Band Beacon Receiver, a space-based radar system, required a programmable radio frequency source to generate local oscillator signals to down-convert the target signals. The Applied Physics Laboratory developed a high-speed direct digital synthesizer system to function as the programmable radio-frequency source. It operates at a clocking frequency of 600 MHz and can output frequencies up to 240 MHz in 35-Hz steps. The packaging considerations were unusual because of the weight, size, and clock rate requirements specific to this application. To accommodate circuit performance at high speeds, the Laboratory used a low-temperature co-fired "green tape" ceramic substrate material with a low dielectric constant.

INTRODUCTION

Preliminary design work on the Mid-Course Space Experiment (MSX) S-Band Beacon Receiver established that a direct digital synthesizer (DDS) was the most efficient method (in terms of power consumption, space, and frequency resolution) for developing a programmable frequency source for space applications. The DDS was to provide a variable frequency output in the 100- to 170-MHz range for up-conversion to 2500 to 2570 MHz for the first local oscillator signal in the Beacon Receiver. The DDS was to be controlled by an onboard digital processor that varies the input control bits to generate the required output frequencies.[1]

The spacecraft environment required that the direct digital synthesizer be compact, power-efficient, able to survive several years in an environment with temperature extremes from −29 to +66°C, able to withstand a high dose of radiation, able to go through many cold and/or hot power-up sequences, and able to operate at a clock speed of 600 MHz.

At the start of the program in late 1989, all of these spacecraft requirements dictated a state-of-the-art advancement in design. A ceramic chip module approach was chosen for development as APL's first space-qualified high-speed DDS. Laboratory personnel selected a low-dielectric-constant (K), low-temperature co-fired ceramic (LTCC) dielectric material manufactured by DuPont (845 Au Tape System).

The dielectric constant of the ceramic substrate material is about 4.8 and the loss tangent is less than 3% over the 5-kHz to 5-GHz range. The material is a glass ceramic made from standard alumina powders and glass and fired at a low temperature, which permits the use of high-conductivity materials such as gold, copper, and silver. The fired dielectric has a flexural strength of about 240 MPa, compared with about 550 MPa for conventional alumina ceramic. The thermal conductivity (2.0 W/m·K) is about one-tenth that of alumina. Multichip modules using high-power devices require the inclusion of thermal vias beneath the hot chips for heat conduction. The temperature coefficient of expansion for the fired material is 4.5 ppm, which is extremely desirable for attachment to often used electronic packaging materials such as Kovar or molybdenum that have low coefficients of expansion.

The basic building blocks of the DDS are primarily gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) devices including a phase accumulator, sine read-only-memory (ROM), and a digital-to-analog (D/A) converter. GaAs technology until now has seldom been used in space applications. The technology adapts itself well to space applications because of its compact size and its inherent high-speed capability; it can also dissipate more power and withstand higher junction temperatures than silicon technology, and can withstand more than 1 Mrad total radiation dose.

Because GaAs MMIC's are a relatively new technology for space uses, no established industrial or military standard exists for quality assurance. Therefore, to demonstrate the suitability of GaAs technology for high-reliability space-borne electronic applications, the completed DDS units were subjected to extensive qualification processes that included electrical, burn-in, life, and stress tests.

THEORY OF OPERATION

The direct digital synthesizer (Fig. 1) consists of four elements: a phase accumulator, sine ROM, D/A converter, and an output smoothing filter. The DDS generates radio frequency (RF) output signals in relation to a specific

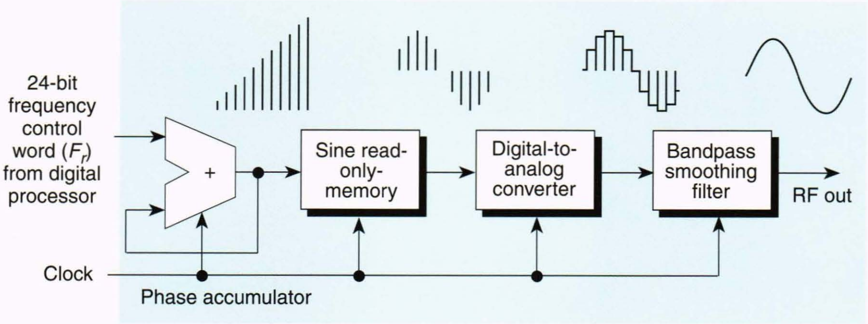

Figure 1. The four elements of the direct digital synthesizer system hybrid.

sequence of events. A 24-bit frequency control word (F_r), which represents the incremental phase change per clock cycle of the output waveform, is loaded into the increment register of the phase accumulator. The frequency control word is updated serially at a rate of 24 Hz with a peak rate of 100 kbps. The frequency control word is transferred between the digital processor and the DDS in two phases. During the first phase, the entire frequency control word is transferred to the DDS in a serial sequence of bit transfers. The DDS interface circuit accepts each bit of the frequency control word and builds the word in an internal register. After the entire frequency control word has been transferred into the DDS and the appropriate clock timing signal has been received, the second phase of the transfer requires that the DDS load the frequency control word into the phase accumulator increment register synchronously with the DDS phase adder clock, so that there is no phase discontinuity in the DDS output. The transfer timing is controlled by the transfer strobe, and the data are sampled on the strobe falling edge. The strobe is gated at the digital processor side so that only twenty-four pulses of the strobe occur per word transfer. The update-enable signal gates the transfer strobe and data, and controls the phase accumulator register loading.

The frequency control word represents the incremental phase change per clock cycle of the output waveform. The phase accumulator adds this value to its present state at each clock cycle, and periodically overflows at the system equivalent of 2π radians; thus, its output is a linearly increasing phase train $\Phi m(kT_{\text{clock}})$ modulo 2π, where k is an integer, T_{clock} is the clock period, and m is the width of the phase word. The minimum output frequency is that corresponding to the smallest phase change per clock cycle (the longest period):

$$F_{\min} = (2^{-24})(600 \text{ MHz}) = 35.76 \text{ Hz}.$$

This is also the frequency resolution, since all output frequencies F_{out} must be some integral multiple of $F_{\min}$ as determined by F_r:

$$F_{\text{out}} = F_r \times F_{\min} = \frac{F_r \times F_{\text{clock}}}{2^{24}}.$$

The maximum output frequency is determined by the Nyquist sampling theorem:

$$F_{\max} < \frac{F_{\text{clock}}}{2}.$$

In practice, because of the aliasing of the output signal, the maximum usable output frequency is limited to 240 MHz. This allows enough of a transition bandwidth for the filter to eliminate the out-of-band alias at $F_{\text{clock}} - F_{\text{out}}$.

The phase train addresses a sine ROM look-up table to obtain sine values corresponding to each specific phase. The sine ROM outputs an 8-bit-wide amplitude word to the D/A converter for conversion into an analog signal. The D/A converter output is then applied to a bandpass filter, which smooths the signal by attenuating out-of-band harmonic and spurious signal components.[2]

HARDWARE DESCRIPTION

Figure 2 shows the actual direct digital synthesizer flight hardware for use on the MSX mission flight. This DDS is a redundant system consisting of five separate boards: primary DDS hybrid, redundant DDS hybrid, clock conditioner, output combiner and bandpass filter, and power switching. The DDS hybrid board, which includes all the significant functions of the DDS, consists of transistor-transistor logic, emitter-coupled logic (ECL), and GaAs components in die form. Figure 3 shows a close-up of an actual flight DDS hybrid board. It includes the three major GaAs building blocks for the DDS process: the Gigabit Logic 10G103 phase accumulator, the Gigabit Logic 14GM048 sine ROM, and the TriQuint TQ6114 D/A converter. The dice were mounted onto a multilayer low-dielectric constant ceramic substrate and sealed in a 5.8 × 2.54 × 0.6 cm package.

The clock conditioner board consists of a four-way power splitter, which distributes two clock inputs to each of the two hybrids, and two phase-delay lines, which delay the phase (about 60°) of one of the clock lines to each hybrid. The output combiner and bandpass filter board includes a combiner that is fed by both hybrids (only one of which is operational) and a bandpass filter placed at the output of the combiner that smooths the output of the DDS. The power switching board switches power to the redundant hybrid if the primary hybrid fails. The complete, redundant DDS system was implemented on five circuit boards mounted in a 15 × 9 × 4 cm aluminum housing.[3]

ELECTRICAL DESIGN

Dense digital circuitry with fast rise and fall times requires a substrate medium with the following characteristics: multiple layers for signal conductors and distributed power and ground planes; lines and spaces

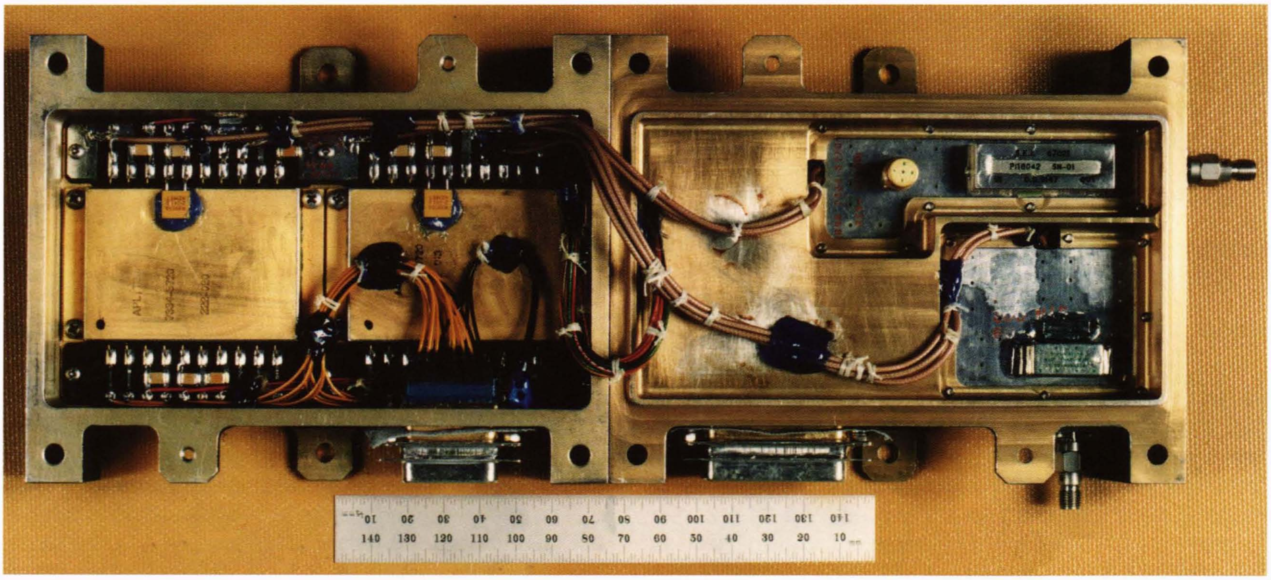

Figure 2. Direct digital synthesizer system flight hardware.

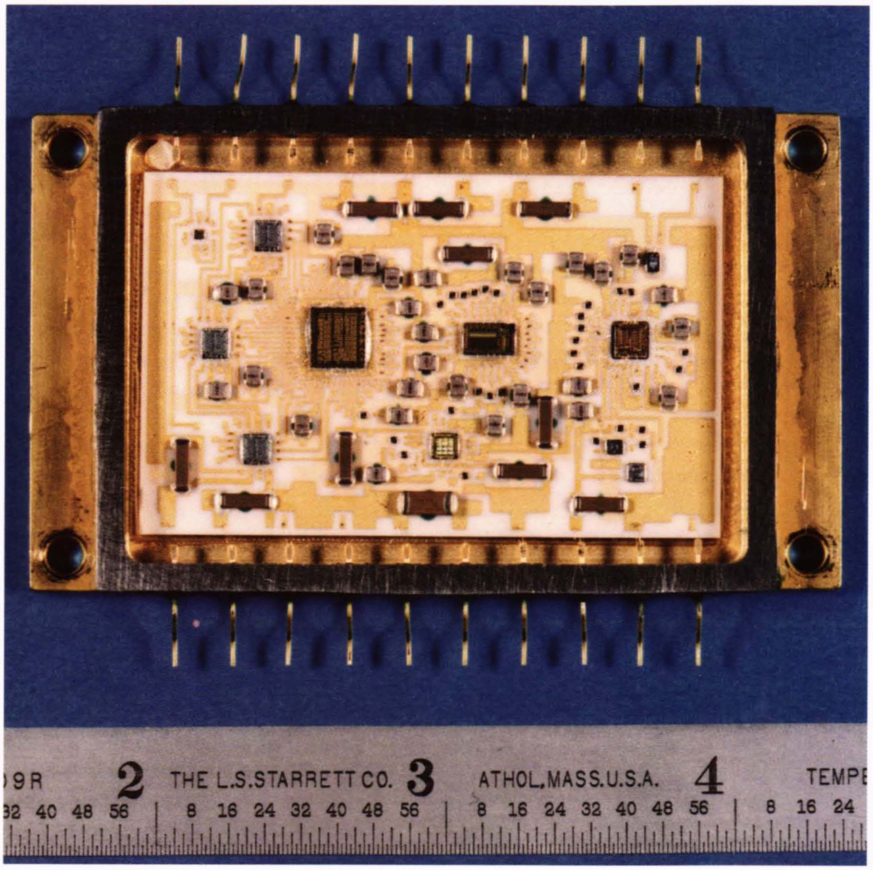

Figure 3. Direct digital synthesizer system hybrid board.

sufficiently narrow to wire high lead-count digital integrated-circuits; low-resistance conductors; low dielectric constant for high-speed pulse propagation; and dielectric layers thick enough to facilitate the construction of 50 Ω transmission lines. Low-*K*, low-temperature cofired ceramic meets all of these requirements.

For high-speed digital pulses, the highest frequency (f) with significant spectral energy can be related to the rise time (t_r) by the approximate relationship

$$f = \frac{0.35}{t_r} .$$

The rise and fall times of the GaAs digital logic used in this design are approximately 150 ps; thus, optimal performance is obtained when the circuitry is designed to be operated at 2.33 GHz.

For frequency components in excess of 1 GHz, transmission line interconnects are required for maintaining signal integrity. Microstrip transmission lines were used for routing signals on the top layer, and dual stripline was used for routing signals on the buried layers. Figure 4 shows calculated values of characteristic impedance for the microstrip lines and the dual striplines, for the dielectric spacing used in the actual DDS low-K LTCC substrate. The characteristic impedance was calculated using a two-dimensional boundary element method,[4] which calculates both the capacitance matrix and the inductance matrix for multiconductor transmission lines, from which the impedance matrix is calculated assuming lossless transmission lines. On the basis of these calculations, line widths of 0.178 mm for the microstrip lines and 0.2 mm for the dual striplines were chosen.

The maximum unterminated length for a transmission line is given by the relation

$$l_c = \frac{t_r}{2T_d} ,$$

where l_c is the critical length, T_d is the substrate propagation delay, and t_r, again, is the rise time. The propagation delays for stripline and microstrip are given by the following relations, respectively:

$$T_d = 0.33(K)^{1/2} \text{ ns/cm}$$

and

$$T_d = 0.33(0.475K + 0.67)^{1/2} \text{ ns/cm} ,$$

where K is the dielectric constant of the substrate. For striplines made with low-K green tape ($K = 4.8$), the unterminated line length is approximately 1.0 cm.

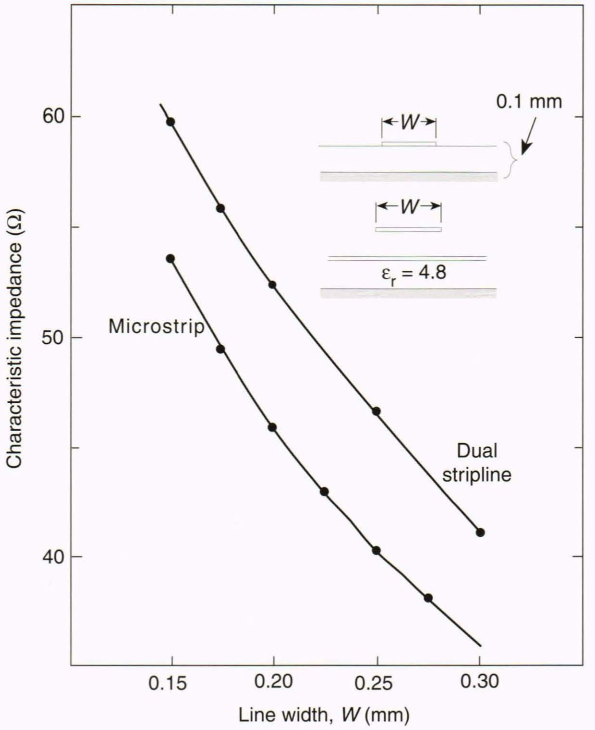

Figure 4. Estimated characteristic impedance values of microstrip and dual striplines for DuPont low-K green tape low-temperature co-fired ceramics.

Cross talk between adjacent, closely spaced conductors carrying fast pulses was also analyzed. Density considerations required that signal lines be spaced no more than two line-widths apart. There was some concern that voltage coupling between adjacent conductors might affect performance. Figure 5 depicts the model for the coupled two-line system used for the analysis. The method of normal modes was used in conjunction with the multipurpose network analysis program SPICE to perform the cross talk analysis,[5] the results of which are shown in Figure 6. The cross talk was estimated to be less than 5% of the voltage swing on the gallium arsenide devices.

THERMAL DESIGN

A critical aspect of the hybrid DDS was the thermal design. The hybrid module was designed for use in a space-borne electronics system where the primary mode of heat transfer out of the module was via heat conduction. Since the thermal conductivity of the substrate was low, the design required either thermal vias or a cutout in the ceramic to enhance heat conduction from the individual devices to the hybrid package.

Thermal vias used for this design consisted of 0.64-mm vias on a 1.28-mm pitch placed directly beneath the heat-dissipating chips. The thermal vias are made with gold thick-film ink and are filled coincidently with the electrical vias. The cutout in the ceramic is made after lamination of the green tape and before substrate firing.

Thermal analysis indicated that the use of thermal vias was suitable for both the phase accumulator and ROM chips but unsuitable for the D/A converter, which is 106

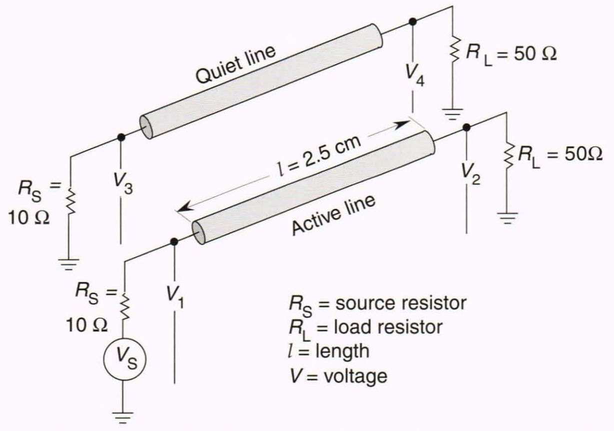

Figure 5. Model for cross-talk analysis of the coupled two-line system.

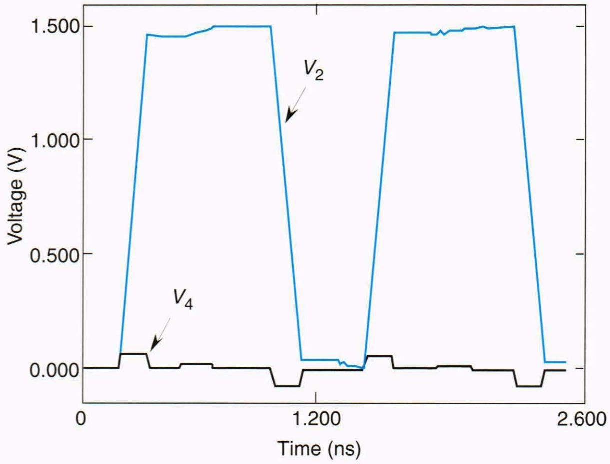

Figure 6. Far-end voltage levels for active and quiet lines using SPICE for the coupled two-line system.

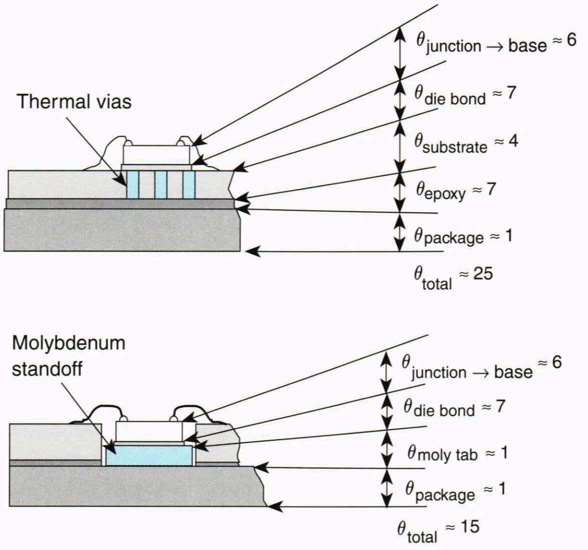

Figure 7. Thermal resistance path for gallium arsenide digital-to-analog converter chip for low-temperature co-fired ceramics (LTCC) with thermal vias and for LTCC with cutout. Thermal resistance θ values are in degrees Celsius per watt.

mils on a side and dissipates 3.5 W. On the basis of hybrid thermal analysis and system operating requirements, the maximum allowable junction to package thermal resistance for reliable operation was 18.6°C/W, thus requiring the use of the cutout option illustrated in Figure 7. A standoff was placed under the chip to facilitate wire bonding and inspection of the die attachment; the standoff used was 1 mm thick, gold-plated, and soldered to the package with gold–tin eutectic solder (melting point 280°C).

Assuming a maximum power dissipation of 15.9 W for the DDS circuitry, preliminary thermal analysis indicated that a standard Kovar package was not sufficient for conducting heat from the DDS module. Therefore, a special hybrid package was designed that consisted of a Kovar lead frame with a high-thermal-conductivity nickel-clad molybdenum bottom. The molybdenum offers excellent thermal conductivity and is a good match for the thermal expansion coefficient of the low-*K* LTCC substrate.

After all of the DDS hybrids were assembled and electrically tested just before lid sealing, the device temperatures were monitored by an infrared thermal imaging camera, which permitted a noninvasive characterization of the thermal design of the unit.

MECHANICAL DESIGN

Low-temperature co-firable glass-ceramics have lower yield strengths than the alumina used in conventional thick- and thin-film electronic applications. As with bonding ceramic substrates to hybrid packages, care must be taken either to maintain the LTCC substrate in a state of compression or to maintain tensile stresses of less than 10% of the fracture strength of the material. Subcritical crack propagation, a phenomenon observed in most ceramic materials, would also be expected to occur in LTCC materials.[6] Also, if not processed optimally, multilayer LTCC substrates can contain voids that may serve as stress concentrators, significantly lowering the fracture toughness of the material. Since ceramics in tension propagate cracks well below the intrinsic fracture strength of the material, substrates should have thermal expansion coefficients properly matched to the other materials, so that when bonded to those other materials they are maintained in compression. Molybdenum is a good choice for the package bottom since it has both high thermal conductivity and a thermal expansion coefficient slightly higher than that for the low-*K*, LTCC substrate.

LTCC SUBSTRATE FABRICATION

The DDS substrate has ten conductor layers constructed on ten ceramic layers. The tape is cut from a roll and then blanked into squares (with registration pinholes and via hole patterns formed all in one step) using a carbon dioxide industrial processing laser. Via holes range from 0.25 to 0.64 mm in diameter for electrical and thermal vias, respectively. The vias are filled with gold conductor paste using a conventional thick-film printer with a Kapton screening stencil. After the via fill layer is dried, the conductor layer is then screened over the vias using a similar thick-film gold paste and a fine mesh stainless steel screen. Each layer is separately laser drilled, via-filled, and conductor-printed. After the paste has been dried, the layers are collated and registered on an alignment plate and placed in a vacuum plastic bag for isostatic lamination. The laminated layers are then placed in an air-vented box oven and heated to 500°C to burn off the organic binders. The resulting block is subsequently fired to a peak temperature of 920°C in a conventional thick-film furnace in an air environment, from which it emerges as a monolithic ceramic multilayer circuit structure. Finally, a laser cuts the circuit to its final size. After substrate fabrication, the completed substrate is tested for continuity and short circuits.

CIRCUIT ASSEMBLY

The completed substrate is delivered to assembly, where it is mounted into the package; components are attached to the substrate, and the devices are wired to bonding pads. Before the substrate is bonded into the package, a small molybdenum tab, used as a heat sink for the D/A converter die, is soldered to the bottom of the package using a high temperature gold–tin solder. The LTCC substrate is then attached with epoxy to the package. After the substrate is epoxy-bonded to the package, all electronic devices, including active dice, silicon chip resistors, and ceramic chip capacitors, are attached to the surface of the substrate using combinations of both conductive and nonconductive epoxies. After the epoxy is cured, the die and silicon chip resistors are wire bonded using 25-μm-diameter gold wire. Wire bonds are also made from the inputs and outputs on the substrate to the gold-plated Kovar pins on the package. After the circuitry has been electrically tested, the package is baked out in a vacuum oven at 125°C for 24 hours and the lid is sealed using a resistance seam welder in a nitrogen-purged atmosphere.

ELECTRICAL SPECIFICATIONS

The DDS is programmed to output a signal in the 100 to 170 MHz range with a resolution of 35.76 Hz. A significant requirement is that the DDS have spurious outputs at least -36 dBc (decibels below carrier) in the scanwidth of 100 to 170 MHz, and -60 dBc from DC to 85 MHz and from 185 to 1300 MHz. The output power must be greater than -5 dBm (decibels above 1 mW) with a stability of ± 1 dB. A 600-MHz clock drives the DDS with an output power of 8 dBm and a power stability of ± 1 dB; the spectral purity of the DDS signal is a function of the input clock, so the clock parameters (i.e., residual phase noise and spurious outputs) were specified with sufficient margin to achieve this goal. The phase noise was specified to be at least -48 dBc in a 1-Hz bandwidth at any offset frequency from 250 to 50 kHz. The spurious and harmonic outputs were specified to be at least -48 and -20 dBc, respectively. The bandpass filter characteristics were restricted by size and weight to a twelve-pole lumped-element Chebyshev filter. The filter parameters were chosen to provide the maximum attenuation possible outside of the passband (a minimum of 60 dB from DC to 70 MHz and from 260 to 650 MHz) and to provide minimum insertion loss (less than 1 dB) and amplitude variation (0.3 dB) in-band.[7]

ELECTRICAL, QUALIFICATION, AND ENVIRONMENTAL TESTS

All parts used in the DDS were purchased already screened to MIL-STD-883 or better, except for the gallium arsenide components in the DDS hybrid. Therefore, the DDS hybrid required extensive testing beyond the standard tests performed on hardware for space use. The risk of using GaAs technology in space was realized early in the development of the DDS, and although data suggested that GaAs components could perform quite well in a space environment, no standards for GaAs MMIC components existed; therefore, no formal component qualification could be implemented. A plan was generated to perform various reliability tests: extensive electrical tests on prototype units, including spectral and current measurements over several temperature cycles; electrical and burn-in tests on the flight hybrids; and a life and stress test to gain insight into failure mechanisms and modes of the DDS hybrid. The resources necessary to build each hybrid, coupled with schedule and budget constraints, limited electrical tests, environmental stress screening, and burn-in tests to fifteen flight DDS hybrids; life tests were performed on five flight DDS hybrids.[8]

All fifteen DDS hybrids underwent preliminary electrical tests in a custom-built test fixture to determine actual performance. At the end of the tests, the data were analyzed and the hybrids were classified in terms of best performance characteristics. Of the fifteen hybrids, two were chosen as the flight hybrids, two were selected for standby, two were classified as spares, five were life tested, and the remaining four were classified as rejects.

Environmental Stress Screening and Burn-in Tests

After the hybrids were sealed, a series of environmental stress screening tests were performed in accordance with MIL-STD-883. The sequence of these tests is shown in Table 1.

The hybrids were burned-in in an oven (Table 1, step 7) at a baseplate temperature of 85°C for 168 h. That temperature corresponds to junction temperatures of about 135°C for the GaAs devices.[9] The burn-in was done at 85°C because it was deemed sufficient to screen out early failures without overstressing the flight parts. Currents were monitored to detect any variation that could constitute an anomaly. At the conclusion of the burn-in test, an electrical test was performed on all of the hybrids and the results were compared with data collected on the hybrids before burn-in. The two hybrids with the best performance characteristics were chosen for the flight unit; the DDS module requires two hybrids (one operational and one spare). The chosen hybrids were integrated with the rest of the DDS components and underwent vibration and thermal vacuum tests. The vibration test subjected the DDS to vibration levels expected during the launch of the MSX spacecraft. The thermal vacuum test

Table 1. Test sequence for the direct digital synthesizer hybrids.

Step	Test type	Method
1	Fine leak	MIL-STD-883, 1014
2	Gross leak	MIL-STD-883, 1014
3	Centrifuge	MIL-STD-883, 2001/B
4	Temperature cycling	MIL-STD-883, 1010/B
5	Particle impact noise detection	MIL-STD-883, 2020/B
6	Electrical	APL TEM-92-327
7	Burn-in	MIL-STD-883, 1015
8	Electrical	APL TEM-92-327
9	Gross leak	MIL-STD-883, 1014
10	Fine leak	Krypton 85
11	X-ray	MIL-STD-883, 2012
12	Vibration	APL S3M-2-1283
13	Thermal vacuum	APL S3P-2-215
14	Electrical	APL TEM-92-318

consisted of six thermal cycles with temperature extremes of 66°C for the hot soaks and −15°C for the cold soaks. A final electrical test was performed at the conclusion of the thermal vacuum test.

Electrical Tests

The two flight DDS hybrids were integrated with the rest of the DDS components and underwent electrical tests during and after each environmental test. The electrical test setup (Fig. 8) consisted of a computer that controlled the settings of the programmable power supplies (−3%, nominal, +3%) and also commanded the DDS interface board; the DDS interface board generated the frequency control words for the DDS hybrids. An HP 8660C signal generator provided a 600-MHz clock signal and an HP 8566 spectrum analyzer monitored the output.

The following electrical measurements were taken for each DDS hybrid at three temperatures (−29, 25, and 66°C) and three voltage settings (−3%, nominal, and +3%) on each of the three power supplies: (1) current output of each supply, (2) power output and stability of each frequency tested, and (3) spurious outputs of each frequency tested. Input and output return loss and phase noise measurements were taken at ambient temperature.

Table 2 summarizes the measurements. Both DDS hybrids met or exceeded all of the electrical specifications.

One concern with the operation of the DDS was the ability to suppress in-band spurious outputs. Since the only filtering is provided by the bandpass filter, any in-band spurious signals appear at the output unattenuated. Those spurious outputs are a function of the frequency selected, depend on the bit settings, and are worse in the upper range of the DDS frequency output capability. As mentioned previously, the DDS has a frequency resolution of 35.76 Hz and therefore can output approximately two million frequencies. Since it would have been impossible to look at all of the frequencies, it was decided to choose frequencies that would yield a high, in-band, spurious output content. Fourteen frequencies were examined ranging from 100 to 170 MHz in mostly 5-MHz steps. Table 3 summarizes spurious performance. The spurious amplitude levels increased at the low temperature extreme and at the higher frequencies. Figure 9 shows the spectrum for an output frequency of 170 MHz and a frequency span from 90 to 180 MHz. As can be seen, the highest spurious level is at −47.9 dBc. The worst spurious levels were recorded in the frequency range of 150 to 170 MHz with levels ranging from −46 to −39 dBc.[10]

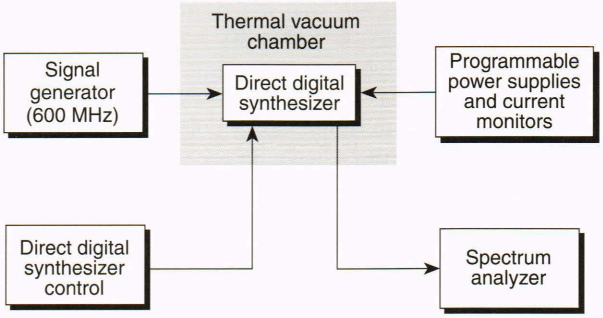

Figure 8. Direct digital synthesizer test setup. The DDS was tested in a thermal vacuum chamber. A computer controlled the DDS and the programmable power supplies.

Table 2. Summary of measured electrical test results.

		Direct digital synthesizer	
Parameter	Specification	Hybrid 1	Hybrid 2
Frequency resolution (Hz)	35.76	35.76	35.76
Harmonics and spurious signals (dBc)	≤36.0	≤ 39.6	≤ 41.0
Output power (dBm)	≥5	≥ 2.3	≥ 2.5
Output power stability (dB)	±1.0	±0.8	±0.9
Residual phase noise (dBc)	−54	>102	>102
Output signal return loss (dB)	>10	>16	>17
600-MHz input return loss (dB)	>10	>14	>14

Note: dBm = decibels above 1 milliwatt.
dBc = decibels below carrier.

Table 3. Summary of in-band spurious performance over temperature (worst case).

	DDS hybrid 1		DDS hybrid 2	
Frequency tested (MHz)	Freq. (MHz)	Level (dBc)	Freq. (MHz)	Level (dBc)
102.500000	177.5500	−53.8	132.5000	−51.5
107.500000	172.4500	−53.6	152.4000	−53.6
112.500000	150.0000	−45.3	187.5000	−49.5
117.500000	129.9000	−50.5	142.4000	−53.1
122.500000	157.4500	−49.2	157.5000	−51.1
127.500000	112.5000	−51.4	112.5000	−52.5
132.500000	147.4000	−51.1	147.4000	−49.0
137.500000	162.4500	−48.8	162.5000	−49.8
142.500000	172.5000	−44.9	112.5000	−45.5
147.500000	137.5000	−39.7	137.5000	−43.1
149.999965	149.9998	−41.0	149.9998	−41.5
150.004900	150.0200	−40.4	150.0200	−41.0
152.500000	162.5500	−39.6	162.5000	−41.6
170.000000	150.1000	−49.6	109.8000	−49.1

Out-of-band spurious outputs include harmonics and the clock feed-through. Measurements taken before integration of the hybrids with the other DDS components (i.e., without an output bandpass filter) show that the highest-level harmonic component is that caused by the clock feed-through signal mixing with the output frequency. This level is usually around −9 to −15 dBc. The amplitude of the clock frequency is also present at about −45 dBc. Several other significant spurious outputs are present (all below −20 dBc) owing to the mixing of the clock harmonics with the output signal harmonics; however, all of the spurious output levels are low enough that when the output signal is passed through the bandpass filter all of the spurious levels are well below the specified −60 dBc.

The power consumption of the DDS varies as a function of temperature and frequency. During the environmental tests, the current variation was recorded for a fixed frequency of 150 MHz (Table 4). The hybrids are most efficient at the low temperature extreme with power consumption around 9.5 W. The power consumption increases to 11 W at a baseplate temperature of 66°C. During preliminary electrical testing of all fifteen hybrids, extensive current measurements were taken for many different frequencies, and the power consumption was never more than 11.3 W; this was significantly less than the original power budget of 13 W.

All three major components on the DDS hybrid (the phase accumulator, the sine ROM, and the D/A converter) were very sensitive to power supply variations. The flight hybrids were tested with power supply variations of ±3% (they were not tested for variations greater than ±3%). Previous tests showed that, with the exception of the −2.0-V supply, the hybrids could tolerate variations in excess of ±5%. Tests also showed that the −2.0-V supply, which powers the phase accumulator, was very sensitive and barely tolerated ±3% variations. Changes in the −2.0 voltage greater than ±3% caused the spurious levels to increase until the DDS ceased to function.

The DDS requires two ECL clock inputs: one to the phase accumulator and one to the D/A converter (delayed by about 60°). Analog-to-ECL converters are used to provide the proper interfaces. The DDS is not very sensitive to the amplitude of the input clock; it functions properly for clock input levels (measured at the input of the four-way power splitter) to −5 dBm. The output level of the clock is such that it provides a margin of about 13 dB.

The amplitude stability of the output signal was also monitored closely. The DDS exhibited amplitude variations over frequency and temperature. Table 5 shows the signal power level performance. The amplitude varies as a function of power supply voltage setting as well as frequency and temperature. The variations over temperature and power supply voltage setting are very minor (0.1 to 0.2 dB), whereas the variations over frequency are as high as 1.6 dB. These numbers include the bandpass filter ripple of about 0.3 dB.

The residual phase noise for the DDS was measured at 25°C with the actual 600 MHz clock used in the spacecraft. Table 6 shows the residual phase noise for the 170-MHz output (worst case). The phase noise margin is greater than 40 dB.

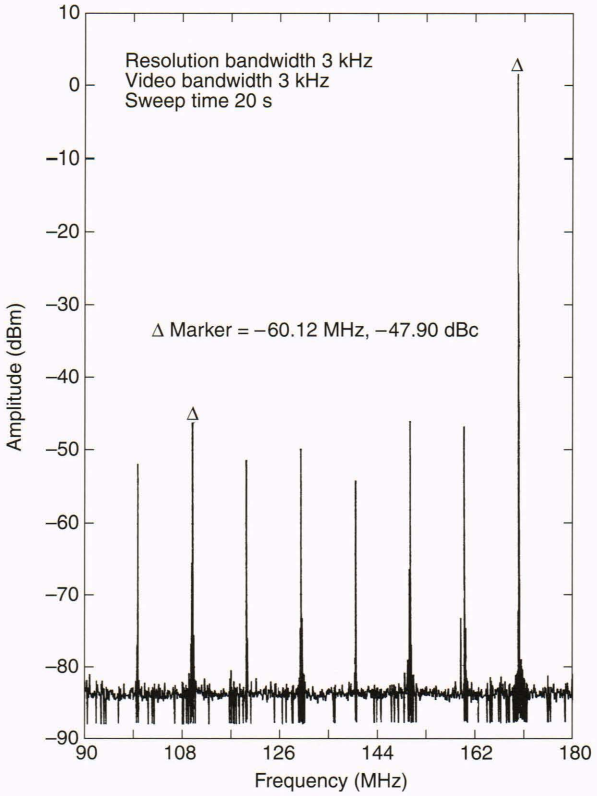

Figure 9. 170-MHz direct digital synthesizer output and spurious outputs (90- to 180-MHz span).

Table 4. Current (mA) and power variation over temperature and power supply settings.

	DDS hybrid 1		DDS hybrid 2	
Voltage	Min.	Max.	Min.	Max.
−12.00	54.7	55.80	54.6	55.7
−8.75	300.7	307.30	304.0	309.9
−5.20	508.0	571.85	23.4	582.5
−3.75	4.8	24.00	6.9	25.7
−3.40	733.7	928.80	737.8	873.0
−2.00	285.1	486.00	203.9	498.0
−5.00	87.9	108.90	95.6	108.8
Total power (W)	9.45	11.10	9.46	11.00

Table 5. Output power levels and variation over temperature.

	DDS hybrid 1			DDS hybrid 2		
Temperature (°C)	Min. (dBm)	Max. (dBm)	Variation (dB)	Min. (dBm)	Max. (dBm)	Variation (dB)
−15	−1.9	−0.8	1.1	−2.0	−0.7	1.3
+66	−2.4	−1.2	1.2	−2.5	−1.3	1.2
Ambient	−2.0	−1.0	1.0	−2.2	−1.1	1.1
Overall	−2.4	−0.8	1.6	−2.5	−0.7	1.8

Table 6. Summary of phase noise measurements (dBc) for the DDS at 170 MHz output.

Frequency offset	Hybrid 1	Hybrid 2
100 kHz	−97	−96
10 kHz	−102	−103
1 kHz	−105	−105
100 Hz	−102	−103
10 Hz	−92	−92
1 Hz	−84	−83

Life Test

Five hybrids were selected for a life test. They were installed in a custom-designed test fixture and the test fixture was placed in an oven with a nitrogen atmosphere. Power was provided by two linear power supplies with linear regulators and over-voltage and over-current protection. The baseplate temperature of the test fixture was maintained at 76°C, a level that provides about 10° of margin over the highest baseplate temperature expected in the spacecraft. Current measurements were taken twice a day during the first 500 hours of the test and once every two days thereafter. The life test lasted 1220 hours, about six times longer than the expected in-orbit usage of the hybrids. All five hybrids survived the life test.

A performance test was conducted for each hybrid that was life-tested. The results of the post-life performance tests were compared with the pre-life test performance test results. In general, there were no appreciable changes in performance for any of the hybrids.

SUMMARY

A high-speed, compact, reliable, and programmable RF direct digital synthesizer system was developed and qualified for space applications using GaAs technology. Extensive testing showed that the DDS system is reliable and exceeds all of the system requirements for which it was designed; test results can be duplicated, and it can survive in a space environment. The DDS was integrated with the Mid-Course Space Experiment S-Band Beacon Receiver during the first quarter of 1993.

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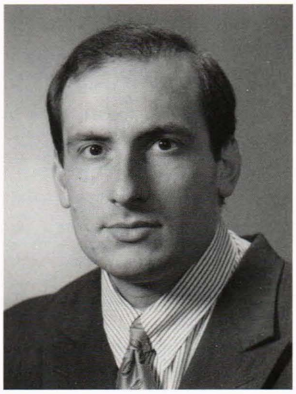

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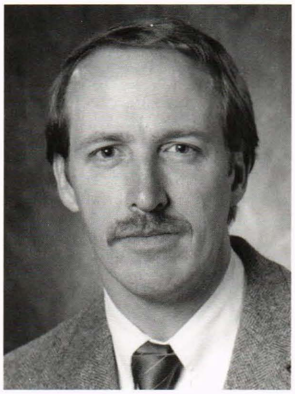

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