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A FOUR-BIT KU-BAND MONOLITHIC MICROWAVE INTEGRATED CIRCUIT PHASE SHIFTER

The Applied Physics Laboratory has recently developed a fully integrated, custom-designed gallium arsenide monolithic microwave integrated circuit phase shifter. It offers considerable size and weight reduction compared with hybrid electronic circuitry where discrete components are placed with printed distributed elements. This article describes the design, analysis, and test results of the phase shifter together with a brief discussion of various generic phase-shifter networks.

INTRODUCTION

Gallium arsenide semiconductor substrates offer an excellent medium for highly integrated microwave circuits, with higher frequency operation potential than with silicon-based integrated circuits. Integrated circuits can drastically reduce the overall size of many systems; they offer better reliability through reduced component interconnects and they are readily mass-produced.

Phase-shifting networks are used primarily in conjunction with phased-array antenna systems to allow beam steering and shaping by electronically controlling the relative phase of the radiating elements. Since phased-array systems are often made up of many elements, it is advantageous to reduce the size, weight, and cost of the electronics supporting each element. Size and weight constraints are increasingly challenging for airborne and space flight systems, where performance improvements are expected along with reduced size and weight. The Applied Physics Laboratory has developed the design tools and expertise to design custom monolithic microwave integrated circuits (MMIC's) for specific program applications where integrated microwave circuitry is needed.

Microwave design engineers at APL have designed a MMIC four-bit phase shifter for operation centered at 13.6 GHz. The phase shifter provides incremental phase steps of 180°, 90°, 45°, and 22.5° to cover the range of 0° to 360° in 22.5° steps. The phase shifter design evolved from an embedded switch high-pass/low-pass topology and was simulated and laid out on a personal computer. Triquint Semiconductor performed the fabrication. The design was optimized for minimum amplitude variation among different phase states within a bandwidth of 320 MHz, and is bidirectional for transmit/receive module applications. APL tested the fabricated phase shifter on a probe station; with subsequent simulations, the phase shifter modeling was improved to better correlate with the test results.

DESIGN APPROACH

Past articles describe several types of solid-state, electronically controlled phase-shifting circuits.[1,2,3,4] Figures 1 and 2 show the basic types of phase-shifting circuits suitable for planar realization. The switched-line phase shifter (Fig. 1A) operates by simply switching between two transmission lines of different physical lengths to provide a relative change in electrical length (insertion phase). This type of phase shifter provides a monotonic phase change with frequency change and has a constant time delay with frequency change. It is often the simplest to implement, but the physical length of the transmission line becomes large where the operational wavelength is large in the planned medium.

Figures 1B, 1C, and 1D show three variants of a reflective phase shifter, where a "movable" short circuit controls a change in phase through the circuit. The first (Fig. 1B) relies on a circulator to direct the signal energy down a transmission line to a short circuit, which reflects the energy back to the circulator. The circulator then directs the reflected energy to the output port with a variable total phase length based on the location of the short circuit. The phase shifter requires half as much transmission line length as the switched-line phase shifter because of the two way travel along the transmission line. This is the only phase shifter described here that is unidirectional and requires a circulator.

The second type of reflective phase shifter (Fig. 1C) uses a 3-dB hybrid power splitter to direct half the signal energy down each of two transmission lines with short circuits. The reflected energy recombines in phase at the output port, giving a variable phase delay based on the location of the short circuits on the transmission lines.

Another variant of the reflective phase shifter (Fig. 1D) uses a 3-dB hybrid with multiple short circuits that can be applied at regular intervals along the transmission lines to provide more than two phase states from a single 3-dB hybrid. Each of the three reflective phase shifters

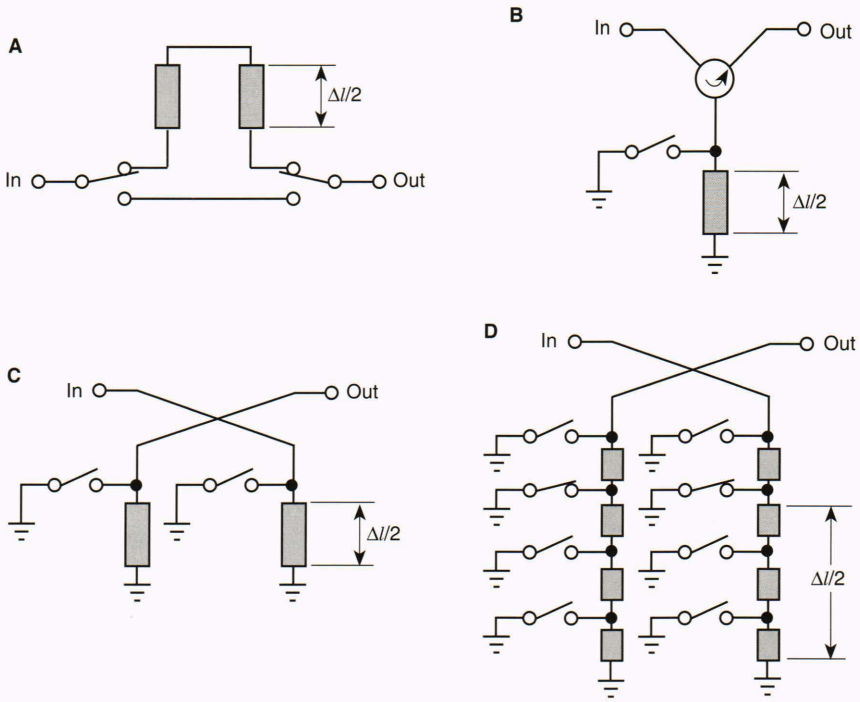

Figure 1. Basic phase-shifting networks utilizing transmission line sections to alter the physical and electrical length of the signal path. In each phase shifter, the net physical path length change is denoted by $\Delta\ell$ and the resulting electrical length change is $\Delta\phi = 2\pi\Delta\ell/\lambda$. **A.** Switched-line phase shifter. **B.** Reflective phase shifter with circulator. **C.** Reflective phase shifter with power splitter. **D.** Reflective phase shifter with multiple short circuits.

is based on variable-length transmission lines which can become large, and the insertion loss in the 3-dB hybrid splitters can be high. Any mismatch in the circulator or 3-dB splitter can contribute to large phase errors.

A loaded-line phase shifter operates by switching a variable reactance on a transmission line to alter the insertion phase length. If two identical reactive loads are placed at quarter-wavelength intervals on the line, the reflection from the two loads will destructively combine 180° out of phase, resulting in a good input match. Figure 2 shows two variations of a loaded-line phase shifter: one with lumped-element loads (Fig 2A), the other with distributed-element loads (Fig. 2B). The distributed-element variation, using terminated transmission line stubs for the reactive loads, enables a simpler switch to be used to provide either an open circuit or a short circuit to terminate the stub. The stubs transform the terminations into reactive components to operate similarly to the lumped-element loaded-line phase shifter, where the short circuited stubs look inductive and the open circuited stubs look capacitive. Loaded-line phase shifters both require a quarter-wave transmission line, which can be large for some applications.

The high-pass/low-pass phase shifter (Fig. 2C) operates by switching between a high-pass filter and a low-pass filter. Both filters are matched at the operating frequency but have different insertion phase lengths. Low-pass filters provide a phase delay and high-pass filters provide a phase advance; hence, the relative difference between these states gives the desired phase change. For example, a 90° phase shifter is composed of a network that switches between +45° or −45° phase length filters. High-pass/low-pass phase shifters have good bandwidth capabilities, but tend to have more insertion loss.

Designers have used all of the previously described phase-shift networks for various applications in either lumped-element or distributed-element form. Selection of the most suitable phase-shift network depends on the electrical requirements and the intended design medium. The MMIC design is often better suited to lumped-element circuit realizations than distributed-element realizations, because of its small size. At the intended operating frequency of 13.6 GHz, distributed transmission line lengths are excessively long for small MMIC's. A lumped-element realization of the transmission lines is certainly possible, but it would have high insertion loss because of the relatively low quality factor of the elements available in gallium arsenide MMIC's. The high-pass/low-pass phase shifter is the only phase shifter described here that does not rely on transmission line lengths; it is therefore well suited for MMIC's. It also offers the best bandwidth performance, so it was selected as a baseline for the four-bit Ku-band MMIC phase-shifter design.

A limited number of semiconductor facilities offer foundry services for fabrication of customer-designed circuits. Much of the processing involved is highly proprietary, and the sale of in-house-designed MMIC's is generally more profitable to the semiconductor facilities. The foundry service creates an opportunity to obtain a unique circuit tailored to a specific application. We chose the TriQuint Semiconductor foundry process because of our confidence in the APL models to accurately simulate the MMIC elements in TriQuint's process. We use computer models and layout patterns to aid in simulation and integrated circuit layout. The Laboratory and the Whiting School of Engineering microwave program are continually revising these models to accommodate foundry process changes and to extend the useful frequency range.

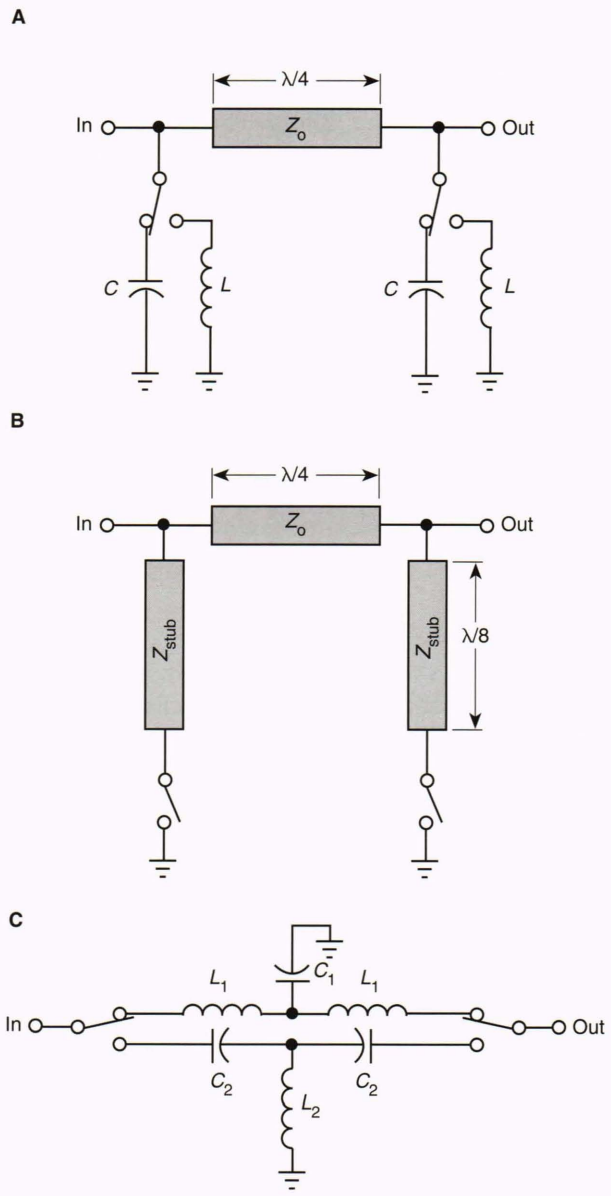

Figure 2. Phase-shifting networks based on reactive elements. The loaded line provides an electrical length change by changing reactive loads on a quarter-wave transmission line. The phase change is $\Delta\phi = 2\arctan[B_N/(1 - 0.5B_N^2)]$, where B_N is the normalized reactive element susceptance. **A.** For the lumped-element case, $B_N = Z_o 2\pi fC = Z_0/2\pi fL$, where C = capacitance in farads, L = inductance in henrys, f = frequency in hertz, and Z_0 = impedance in ohms. **B.** For the distributed element case, $B_N = Z_0/Z_{stub}$. **C.** The high-pass/low-pass network provides a phase change by switching between two filter networks with different electrical phase lengths. The phase change is defined by $\Delta\phi = 4\arctan(X_N) = \arcsin(2B_N)$, where $X_N = 2\pi fL_1/Z_0 = 1/Z_0 2\pi fC_2$, and $B_N = Z_0/2\pi fL_2 = Z_0 2\pi fC_1$.

At higher frequencies, the model parameters need refinement, and additional parasitics must be incorporated into the models. APL and the Whiting School have also developed design rule checking (DRC) software to verify that a MMIC design conforms to the foundry's layout rules and requirements. The semiconductor foundry performs their own DRC on new fabrication designs, but it is much more efficient to sort out any design layout rule violations during the layout phase before submission to the foundry.

Electrical Design

The electrical design of the phase shifter is based on switching between a high-pass filter and a low-pass filter to provide a shift in the insertion phase length. A conventional application might require a network of single-pole, double-throw switches to select between one of the two filters to obtain the desired phase state. The basic circuit (Fig. 2C) is used in lumped-element realizations.

Positive-intrinsic-negative (PIN) diodes are often used in semiconductor switches and phase shifters, but were not available in the chosen wafer fabrication process. Field-effect transistors (FET's) were available that could be used in a switched mode by controlling the gate bias voltage. Figure 3 shows a simplified electrical model for a 300-μm FET with zero volt bias across the drain-source terminals. The depletion-mode FET's available for the design could be biased "on" with a zero volt gate-source bias to put the FET in a low drain-source impedance state. In the low-impedance "on" state, the circuit shown is dominated by the drain-source resistance (R_{ds}). Biasing the gate with negative four volts relative to the source puts the FET in its pinch off mode, or "off" state, where the drain-source impedance is high and the circuit is dominated by the drain-source capacitance (C_{ds}).

When FET's are used to design a switching network, the FET characteristics, which contain resistive and capacitive parasitics, must be modeled and absorbed into the design. The capacitance of the FET in its "off" state is directly related to the FET size (area). The "on" state resistance is definitely not zero and is inversely proportional to the FET size. The electrical model of the FET available in the TriQuint Semiconductor process (Fig. 3) was analyzed with EEsof's Libra microwave simulation software. Figure 4 shows the simulated Smith chart impedance response of 300-μm and 1-mm FET's in the "on" and "off" states. The S_{11} (input return loss) parameter was simulated at the FET drain with a grounded source and would indicate a perfect short at the left side origin, a perfect capacitor anywhere on the lower circumference of the chart, and a perfect open circuit on the right side origin of the chart.

The larger 1-mm FET clearly has the desirable characteristic of lower "on" resistance for lower circuit loss, but is over the practical limit of 360 μm for individual FET's in TriQuint's process. Where larger than 360 μm is required, additional FET's must be connected in parallel, or a new FET layout must be created—risking, however, the ability to predict its response. Therefore, the parallel FET solution was chosen where needed. The resistive losses are the most detrimental aspect of using the FET's in this application. In general, filter response degrades quickly when losses are introduced that lower the circuit quality factor. On the other hand, in the "off" state, the ideal response is an open circuit. The smaller 300 μm has less capacitance and better represents an open circuit. Therefore, the FET size is a compromise between low loss and low capacitance; hence, FET size must be determined through circuit analysis and optimization.

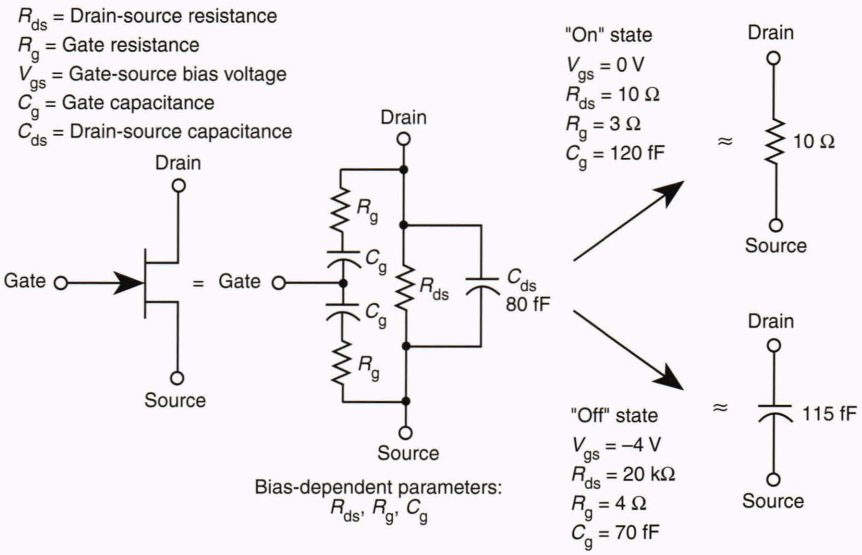

Figure 3. Field-effect transistor (FET) electrical switch model. An FET can be used in a switch mode by altering the gate bias voltage to place the device in a high-conductance "on" state or in a pinched "off" state. The values shown represent a 300-μm FET. The simplified electrical model reduces to a resistor for the "on" state and a capacitor for the "off" state.

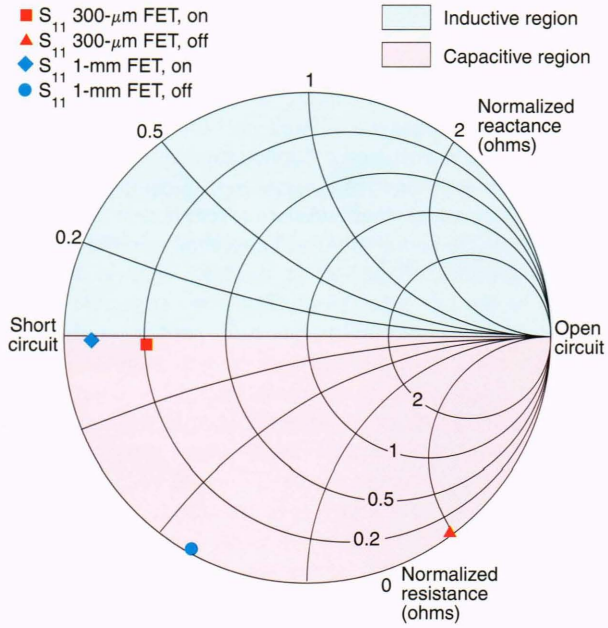

Figure 4. Smith chart representation of field-effect transistor switch impedance. The impedance is simulated at the FET's drain terminal with a grounded source. The "on" state for both size devices lies close to the horizontal axis, indicating that the impedance is nearly purely resistive, with the left side origin indicating a short circuit (zero impedance) and the center indicating a matched load (50 Ω in this case). The "off" state for both size devices is along the lower circumference of the chart, indicating that the impedance is nearly purely capacitive; points closer to the left side origin indicate a lower impedance (higher capacitance).

A variation of the high-pass/low-pass phase shifter, known as an embedded-switch phase shifter, deals with the parasitic capacitance in the FET "off" state by incorporating it into the necessary reactive capacitive elements.[5] Figure 5 shows an embedded-switch phase shifter—approximately equivalent to the high-pass/low-pass filters in Figure 2C–for an FET which is purely capacitive in its "off" state and purely resistive in its "on" state. When the x FET's (Fig. 5) are "off" (capacitive) and the y FET's are "on" (low resistance), the circuit resembles a high-pass network with series capacitance and shunt inductance. Conversely, when the x FET's are "on" (low resistance) and the y FETs are "off" (capacitive), the circuit resembles a low-pass network with series inductance and shunt capacitance. The high-pass network requires a shunt inductance to ground, but there appears to be an inductor/capacitor (LC) resonant circuit in the path to ground. The resonant frequency (f) of the LC network is higher than the operational frequency range, allowing the LC network to "look" inductive. For example, the 22.5° bit has its LC network resonant as follows:

$$f = 1/\left(2\pi\sqrt{LC}\right) = 1/\left(2\pi\sqrt{0.6\text{nH}\cdot 50\text{fF}}\right) = 30\ \text{GHz}.$$

The embedded-switch topology was selected for the four-bit Ku-band MMIC phase shifter design. The more complete FET model shown in Figure 3 was used for computer simulation where the FET losses resulted in further topology adjustments. The detailed circuit design was derived using a personal computer running EEsof's Libra software for analysis and EEsof's Academy software for circuit layout. The starting point in the design was based on the ideal values for capacitors and inductors in a standard high-pass/low-pass lumped-element network. The Libra files were set up for each individual bit with a defined two-port network for each phase state. The two state circuit files were identical except for the transistor parameters, which were set up as variables to allow readily varying the transistor size while optimizing the response. The computer-aided optimization routines were extremely powerful in determining optimum component values, but the design process required considerable manual interaction to control needed changes in the circuit topology. The topology changes were determined by several factors, including foundry process constraints, layout size constraints, and cases where values tried to go to zero or infinity. The standard spiral inductors in the

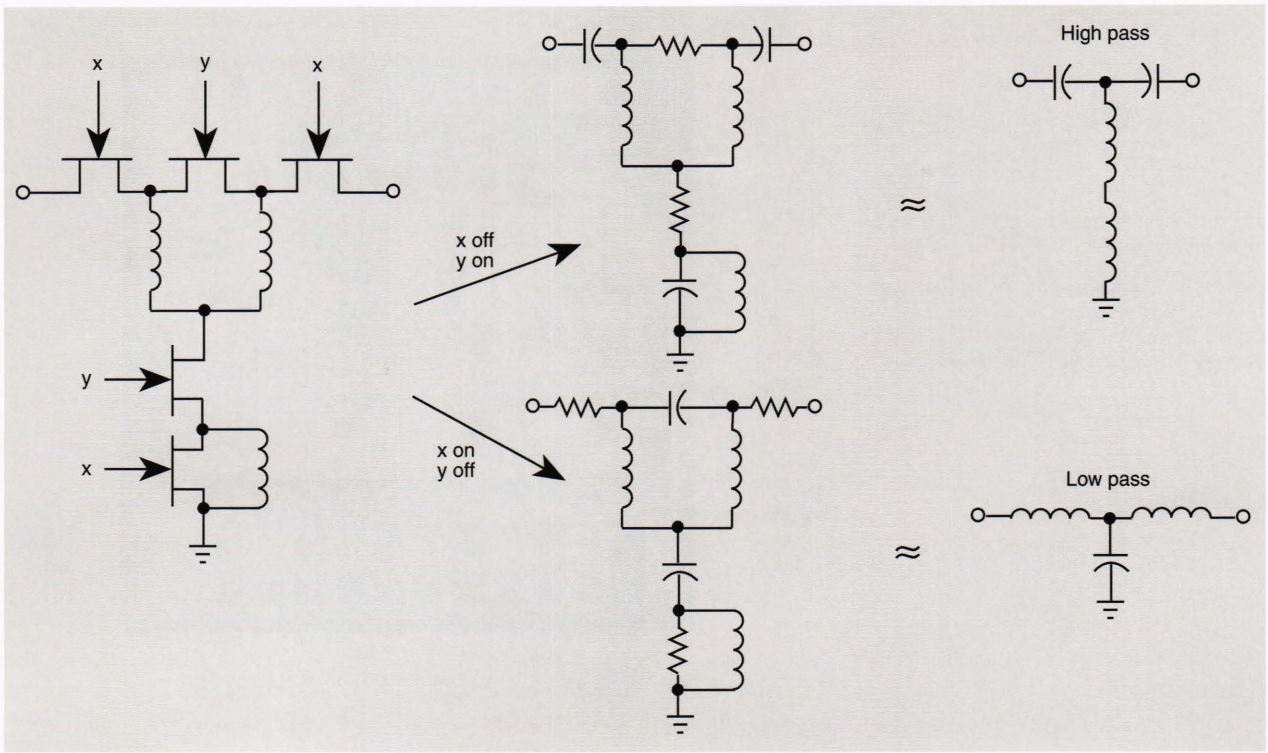

Figure 5. The embedded-switch phase shifter is nearly equivalent to switching between two filter networks. The figure shows the phase shifter network changing to either of two states, with some of the field-effect transistors (FET's) turning on (represented as resistors) and some turning off (represented as capacitors). The resistance of the "on" FET's is a parasitic aspect of a desired short circuit, so they are ignored here for the sake of visualizing the complete transition to the conventional filter network. Another simplification, is where a parallel inductor and capacitor are dominated by the inductance and shown as simply an inductor.

chosen process were available in discrete values, requiring a short variable-length transmission line to allow computerized inductance tuning. When the line grew too long, a higher-value spiral inductor was chosen, and vice versa. In selecting the transistor sizes, the previously mentioned limit of 360 μm necessitated the paralleling of two transistors in some cases.

Each bit initially contained a discrete capacitor in parallel with a transistor to provide capacitance in addition to the transistors' parasitic capacitance. Each of these capacitors was eliminated as the transistors grew larger to reduce the transistors' "on" state resistance up to the limit where their "off" state capacitance reached the required value. The design contains no discrete capacitors except for bypassing at the digital control inputs. During the design optimization, the transistors at the input and output of each phase bit grew extremely large and were simply eliminated as their low "on" resistance and large "off" capacitance became closer to a short circuit for each state. By referring to the Smith chart (Fig. 4), it can be seen that increasing capacitance and decreasing resistance converge to the same zero impedance point.

It seemed at first that the circuit could not work without the FET's providing the series capacitance elements. As the circuit optimization progressed, the individual phase-shifter bits evolved from high-pass/low-pass filters to direct-line/low-pass filters. For example, the 90° bit went from a +45°/−45° phase length to a 0°/−90° phase length. This is somewhat unorthodox, but seemed to be the best solution in dealing with the losses associated with the available elements. Similarly, another FET from the 180° bit was eliminated as the transistor size grew larger.

Layout Design

The MMIC design was laid out on a 0.09-by-0.09-in. chip (Fig. 6). The four phase bits are the 22.5°, 45°, 90°, and 180° phase shifters. The transistors and spiral inductors are clearly visible; in some cases a narrow (5 μm) line is used for inductors of less than 100 pH (where 100 pH is the minimum standard spiral inductor). Coplanar transmission line launches (connections) are placed at the input and output to interface with the test station probes. The coplanar launches connect the return line to chip ground through via holes. At the top of the chip, a level shifting and inverting network receives a transistor-transistor logic (TTL) level single-ended input and generates both the 0 V and −4 V needed to drive the FET gate bias inputs. The bias network uses very small (≈10 μm) FET's, since little current is needed to drive the high-impedance FET gates. Each level shifter with complementary outputs draws 5 mA from a ±4 V power supply and occupies an area of 8 by 10 mils. The FET bias voltages are fed to each FET gate through a series 2000-Ω resistor to reduce possible effects of inductance in the bias line between the transistor and the bias generating network.

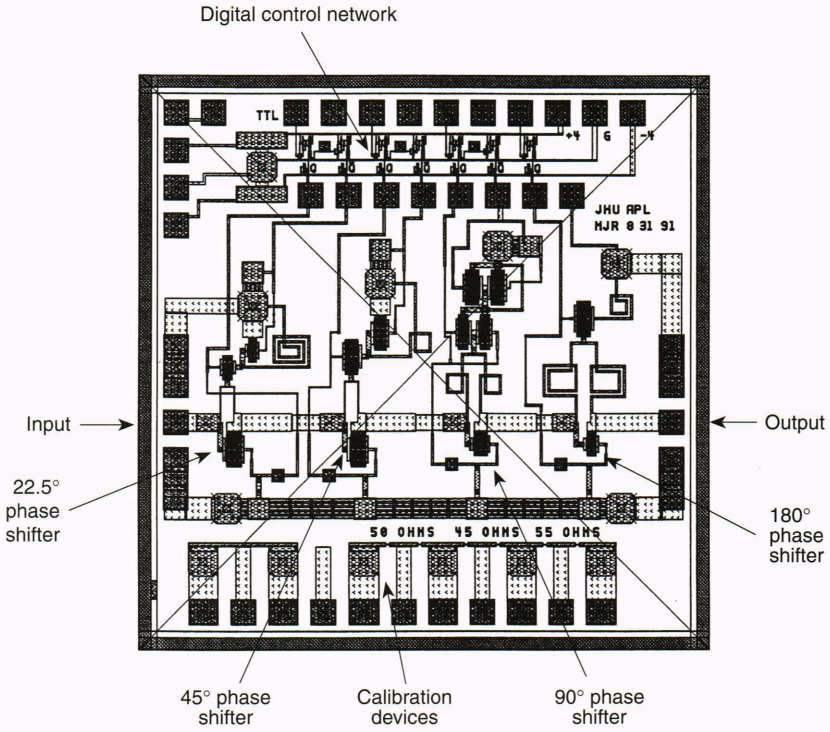

Figure 6. Computer-generated drawing of phase shifter layout showing four cascaded phase-shifter elements and supporting digital bias generating network.

At the bottom of the chip are devices for calibration of the probe station interfaces with a network analyzer. For better characterization, an additional layout was created with the 180°, 90°, and 22.5° bits set up for individual probing without the potential effects of voltage standing-wave ratio (VSWR) mismatches from adjacent phase bits. The layout drawing file was analyzed on a personal computer for conformance with the foundry-specified layout rules. The computer software design rule checking (DRC) routines analyzed several parameters, including conductor line widths and spacing, FET and other device layouts, layer compatibility, and spacing to the edge of the chip. After the initial DRC at APL, the design was submitted to the semiconductor foundry for more complete DRC; no rework was required.

ANALYSIS

The phase shifter was thoroughly analyzed over the band of 13.4 to 13.8 GHz. The sixteen phase states (Fig. 7) were determined to be within 6° of the desired value across the band. Note that the displayed phase is absolute insertion phase, where the relevant parameter is the relative phase from state to state. The 180° bit was the least accurate of the four phase bits because of its limited bandwidth. The topology selected is better suited for smaller phase shifts, but appeared to be adequate for the desired performance characteristics. The amplitude loss through the phase shifter was simulated at 7 dB with only 0.5 dB of variation among the phase states. The worst case VSWR was simulated at 1.6:1 (12.5 dB return loss). The individual phase bits had a better match, but when cascaded, the overall match degraded somewhat, as expected. The VSWR was traded off to optimize the phase shift at the band center to optimize the amplitude balance among phase states.

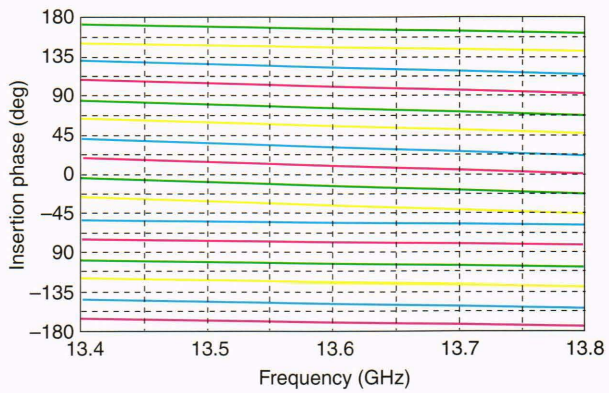

Figure 7. Computer-simulated insertion phase length versus frequency. Sixteen states are shown from −180° to +180° in increments of 22.5°. Phase change is defined as the relative difference between these states.

A sensitivity analysis was performed (in lieu of a yield analysis) with a pass/fail criteria of 5° of phase error at the band center, or with 1 dB of amplitude variation. The 5° phase error criteria turned out to be more stringent than the amplitude variation criteria, and the 180° bit was the most sensitive to element variations. The series pass transistor in the 180° bit was determined to cause 5° of phase shift with a 5% change in size. The next most sensitive bit was the 90° bit, where, similarly, a 14% change in FET size resulted in a 5° phase shift.

A stress analysis was also performed to determine the electrical stress imposed by a peak power level of +10 dBm at the MMIC. The peak current and voltage were determined through computer simulation for each inductor and transistor. The peak current of every inductor was well below the safe limit specified by the semiconductor foundry, and the peak voltages at the transistors were well below the specified breakdown limit. The potential effects of power level on phase-shifter performance were also investigated, where self-biasing of the FET's had to be considered. An analysis was performed to determine where the phase shift was degraded by greater than 5° and where the amplitude variation was greater than 1 dB. The phase shift was not degraded by power levels below 16 dBm. The amplitude compressed at 7.6 dBm in the 90° bit, and although this was below the 10 dBm nominal level, it did not appear to be a serious problem, since the compression was 2 dB at 10 dBm.

TEST RESULTS

The fabricated phase shifter was tested as a bare chip on a probe station and network analyzer (Fig. 8). The probe station (Fig. 9) allowed accurate testing of unpackaged devices, either as part of an entire wafer, or as a single chip. A ten-contact needle probe connected the four TTL control lines and two supply lines to the bias generating network. Several chips were tested with good results. The 22.5°, 45°, and 90° bits worked as predicted over the 13.4- to 13.8-GHz band. The 180° bit was off in frequency with approximately 147° of phase shift at the center of the desired frequency band, but worked well at the higher frequency of 15.7 GHz.

Table 1 summarizes the phase-shift and amplitude-balance results of a measured chip at 13.6 GHz. It also shows the source of the phase-shift inaccuracies in states 1, 2, 4, and 8, where the phase shift should be 22.5°, 45°, 90°, and 180°, respectively, for each individual bit. Another measured four-bit phase shifter gave similar results with better amplitude balance and less overall amplitude loss, but with slightly poorer phase accuracy. The phase shifter summarized in Table 1 had a worst-case 4.6 dB amplitude imbalance with a nominal insertion loss of 8.3 dB. The impedance matches S_{11} (input return loss) and S_{22} (output return loss) were also measured with a worst case of 9 dB return loss (2.1:1 VSWR). The impedance match was much better in some phase states where the multiple reflection waves can add constructively or destructively. Some of the phase-shift bits were tested individually to avoid potential detuning from adjacent phase bit impedance mismatches. Each phase-shift bit worked similarly under these conditions, indicating that the composite VSWR presented to the individual bits had little impact on their operation. The tests also showed the 180° phase bit to be relatively insensitive to bias voltage offsets, thus eliminating the bias network from the possible causes of its phase-shift inaccuracy.

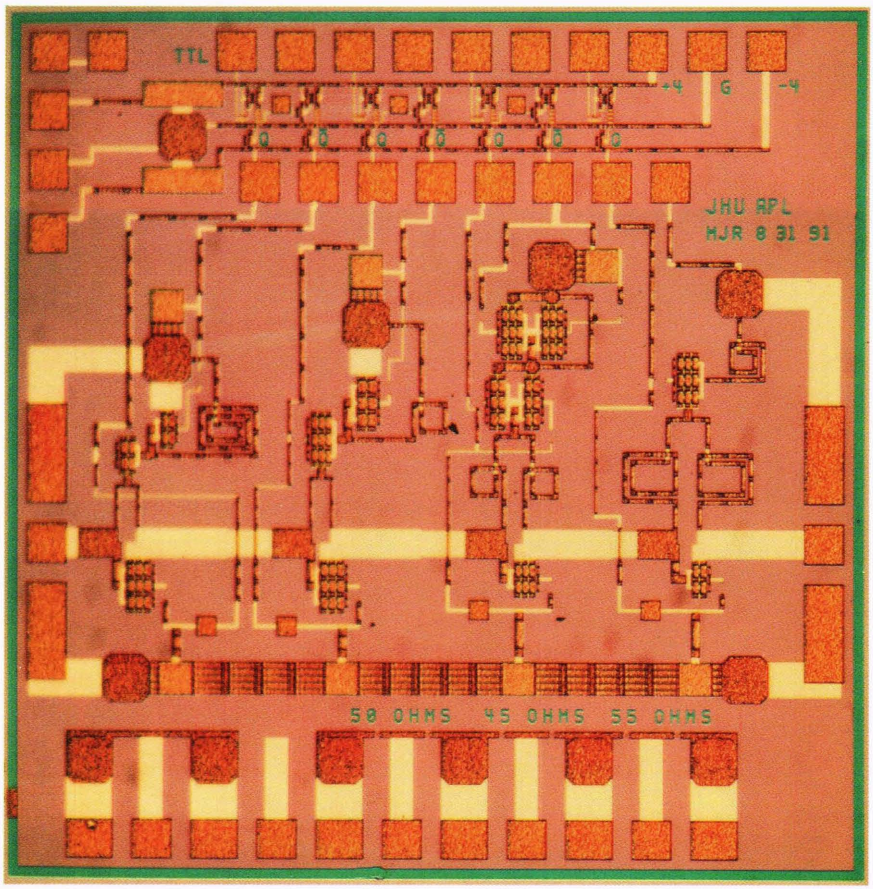

Figure 8. Microphotograph of fabricated phase shifter on gallium arsenide substrate. The circuit measures 0.09 by 0.09 in.

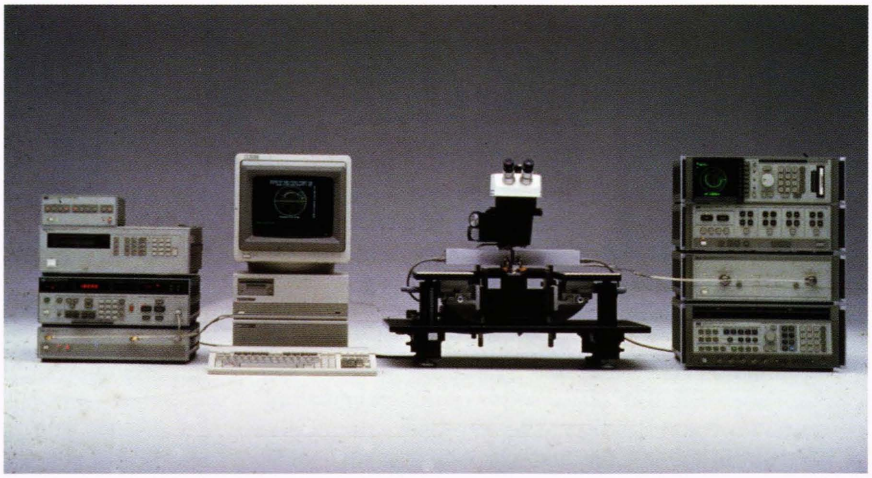

Figure 9. Typical probe station used to test unpackaged monolithic microwave integrated circuits (MMIC's). The microscope is used to manually align the electrical probes with the MMIC chip, and the computer controls the test equipment. The electronic equipment shown includes a network analyzer and noise figure measurement instruments. Reprinted, with permission, from Ref. 7. © 1988, Cascade Microtech, Inc.

Table 1. Measured performance of fabricated chip at 13.6 GHz. The 16 states span approximately ±180° in 22.5° increments.

State	Ideal phase shift (deg)	Measured phase shift (deg)	Amplitude balance (dB)
0	0.0 reference	0 reference	0.0 reference
1	22.5	21	−0.3
2	45.0	42	−1.2
3	67.5	61	−2.0
4	90.0	95	−2.4
5	112.5	113	−2.6
6	135.0	134	−3.1
7	157.5	153	−3.8
8	180.0	147	−1.4
9	−157.5	167 (−193)	−1.8
10	−135.0	−176	−2.3
11	−112.5	−157	−2.9
12	−90.0	−125	−3.2
13	−67.5	−106	−3.3
14	−45.0	−85	−3.9
15	−22.5	−66	−4.6

We also performed tests over the broader band of 9.6 to 17.6 GHz. The 22.5° bit had the best broadband performance and the 180° bit had the worst, as expected. The test did indicate that the three lower phase bits were optimum at the desired center frequency, and the 180° bit was optimum at 15.7 GHz. Where the 180° bit phase shifter crossed the desired phase angle, the amplitude variation was also good at 0.3 dB.

The effect of drive power was also considered in the phase-shifter tests. Tests were run with the network analyzer set to zero and later at a 10-dBm source power. The 10-dB power change produced no noticeable change in phase-shifter performance; however, the actual power at the probe tip was a few decibels less than the source power.

POST-TEST ANALYSIS

Engineers at APL desired better correlation between the 180° bit test results and the computer analysis. On the same wafer that contained the phase shifter, several model verification structures were also present. The model verification structures were measured for comparison with simulated results and some discrepancies were found. The foundry manual originally suggested an FET switch model that was found inadequate in this application. We created a new FET switch model based on measurements of 300-μm and 150-μm periphery FETs. The new switch model changed the predicted phase shift from 180° to 170° at 13.6 GHz. We also considered the interconnecting lines, which we originally simulated as mi-

crostrip lines. The model verification structure tests indicated that the short interconnecting lines could be better simulated as thin-film resistors or simple inductors based on Grover's equations[6] for inductance of rectangular bars. With the new FET switch model and short air bridge interconnects modeled as simple inductors, the phase shifter simulation resulted in a predicted phase-shift of 154°. The coupling between parallel lines spaced 50 μm apart was included as a mutual inductance with negligible influence on the phase shift simulations. We modeled the spiral inductors as suggested by the foundry, but subsequent testing of the model verification structures indicated that better correlation in this frequency range could be obtained by deleting the suggested shunt capacitance to ground, which was added to the inductor ends in the computer simulation. Modification of the inductor model used for simulating the phase shifter, as well as the previous model changes, resulted in predicted phase shifts of 141° at 13.6 GHz and 180° at 15.3 GHz. This correlates well with the measured results of 147° at 13.6 GHz and 180° at 15.7 GHz.

Using updated computer models, APL redesigned the 180° phase-shift bit to center its operation at 13.6 GHz. The redesign required only a change in the inductance values to produce the desired 180° phase change with a ±7° variation across a 320-MHz bandwidth. Another, more conservative, approach considered was to cascade a pair of 90° phase bits for the desired 180° phase shift. The 90° phase bits were verified to work well by characterizing the scattering parameters on a network analyzer. By analyzing the response of two 90° phase bit scattering-parameter files in series, the projected performance of this type of 180° phase shifter was determined. Although this design offers better phase performance and lower VSWR across the frequency band (180 ± 2°), it does occupy more space and have poorer amplitude balance (2 dB). Table 2 shows the projected performance at the center of the frequency band for future fabrication of this second redesign approach.

CONCLUSIONS

The measured performance of the as-built phase shifter agrees with the updated simulated response. In general, discrepancies between measured and simulated results are due to flaws in the circuit layout that did not get simulated, and to processing variations, flaws in the element models, and unmodeled parasitics. The largest discrepancy from the design goals was in the 180° bit, which is centered at a higher frequency than originally expected; the discrepancy arose from the initial simulation model problems. The other three phase-shift bits were less affected by the model changes because their designs had a wider bandwidth. A suggested modification to the phase shifter was presented for future fabrication runs to optimize the performance of the device.

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Table 2. Projected performance of phase shifter at 13.6 GHz.

State	Ideal phase shift (deg)	Measured phase shift (deg)	Amplitude balance (dB)
0	0.0 reference	0 reference	0.0 reference
1	22.5	21	−0.3
2	45.0	42	−1.2
3	67.5	61	−2.0
4	90.0	95	−2.4
5	112.5	113	−2.6
6	135.0	134	−3.1
7	157.5	153	−3.8
8	180.0	179	−2.1
9	−157.5	160	−2.4
10	−135.0	−139	−3.3
11	−112.5	−120	−4.1
12	−90.0	−86	−4.5
13	−67.5	−68	−4.7
14	−45.0	−47	−5.2
15	−22.5	−28	−5.9

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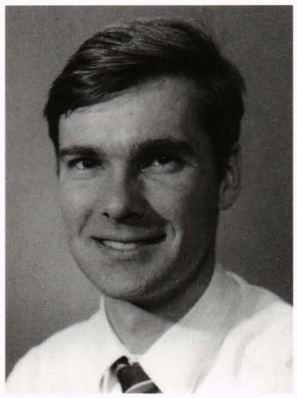

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