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MATERIALS IN ELECTRONIC PACKAGING AT APL

Materials and their proper application are key elements in the creation of high-performance electronic packaging. This article details the use and importance of modern electronic packaging materials and the contributions that the Applied Physics Laboratory has made to advanced packaging materials science.

INTRODUCTION

The rapid advancement of integrated circuits and associated electronics technologies toward complex, high-density, high-speed devices has placed increasing demands on electronic packaging and its materials structures. As digital clock "speeds" exceed 100 MHz and rise times drop below 1 ns, the need for properly terminated transmission lines that preserve pulse shape and minimize propagation delay is paramount. Analog and high-frequency microwave circuits need integrated packaging structures with low loss and wide bandwidth to preserve signal integrity. The increased number of inputs and outputs of chips associated with the exponential rise in chip device density[1] (Fig. 1), and the exponential decline in device and package feature size[2,3] (Fig. 2) for very-large-scale integrated (VLSI) circuits, have forced significant increases in packaging density and made apparent the need for high-conductivity, low-capacitance/inductance interconnects and advanced packaging materials.

Because increased device density and high-speed operation usually imply greater power consumption, more attention must be paid to the overall thermal management and to the reliability and chemical and physical integrity of electronic interconnection, encapsulation, passivation, and packaging materials. All these rapidly changing packaging parameters[4] have created a growing need for advanced materials for device substrates, packages, interlayer dielectrics, passivation, attachment adhesives, encapsulants, package sealants, and interconnections.

Since a myriad of materials are used in electronic packaging both within industry and at APL, this article will

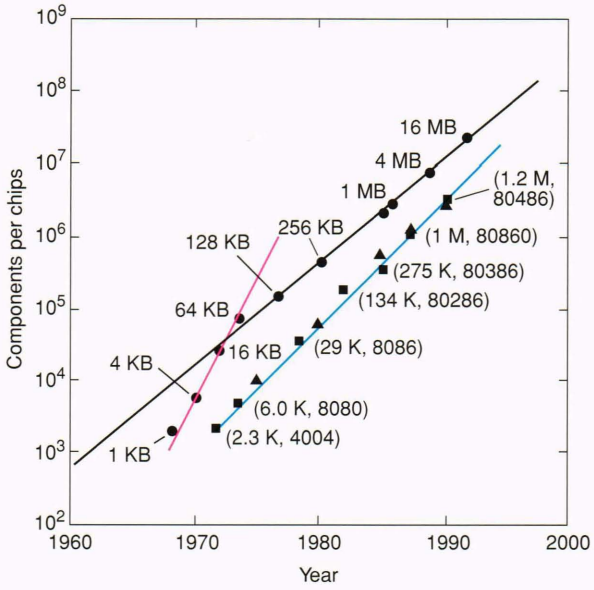

Figure 1. The number of components per chip versus year for three major device categories (dynamic memory [●], microprocessors [■], and random logic application-specific integrated circuits [▲]). The red curve shows the original Moore's law[1] for memory (size doubling every year), the black curve shows the current trend for memory (size doubling every two to three years), and the blue curve shows the current trend for microprocessors and random logic. The data in parentheses refer to typical microprocessor types: the value on the left is the number of transistors on the chip, and the number on the right is the typical microprocessor chip.

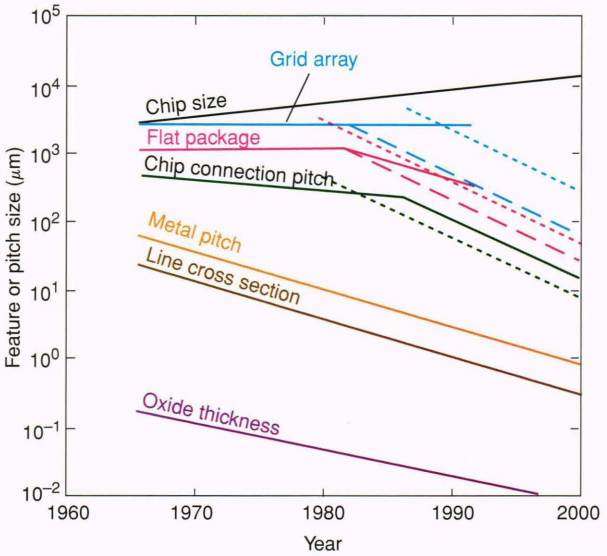

Figure 2. Decrease in size of device, chip bonding, pad, and package input/output features with time. The dashed lines are the single chip in package requirements, and the dotted lines are the multichip module (MCM) requirements. The MCM assumes four chips, 200 input/output, and 50% silicon area coverage. Line cross section refers to the change in line width for a constant 1-mm-thick conductor. Channel length (not shown) parallels line cross section.

focus on general classes of materials (e.g., epoxies, silicones, metals, alloys, and ceramics) and their applications to advanced packaging. Specific APL examples will be presented that emphasize not only the materials and their properties, but also how the proper choice of materials has enhanced circuit performance and long-term reliability. Application areas include single-chip and multichip packaging, board and substrate structures, die (substrate) attachment and electrical interconnection, circuit and board passivation, and encapsulation or package sealing. (Passivation is a process by which a device or substrate is protected against contamination by coating or surface treatment.)

In general, all the materials to be described fall into two broad categories: inorganic and organic. Organic resins filled with inorganic materials (metals and high-thermal-conductivity ceramics) are quite commonly used in die interconnect and attachment, however. Similarly, certain organic vehicles containing inorganic dielectrics are used as overcoats.

Inorganic materials include metals and metal alloys used for attachment, electrical interconnection, and packaging structures. Alumina (Al_2O_3), silicon, aluminum nitride, and beryllia (BeO) have proved most useful for substrates and packages, whereas silicon oxide, silicon nitrides, metal oxides, glasses, and certain ceramics have been used for device passivation and encapsulation. Inorganic coating has been found to be the best for device passivation and hermetic "caps" on integrated circuits.[5]

Organic materials include polyimides and epoxies used for the majority of printed wiring boards (PWB's). Polyimides, epoxies, and thermoplastic and thermoset resins are used for both die attachment and interconnection. Various organic materials are used for coatings and encapsulation; they include epoxies, polyimides, urethanes, silicon polyimides, Parylene (Union Carbide trademark for poly[*p*-xylylene] deposited by the Gorham process), benzocyclobutene, block copolymers, and sol-gels.

DEVICE/CHIP ENCAPSULATION

The Applied Physics Laboratory has maintained a capability to produce device encapsulation and passivation layers for thirty years.[6] In the early years, these activities were focused on the fabrication of semiconductor devices[6] and thin-film hybrid microcircuits.[7] The materials, which included thermally grown silicon dioxide, chemical vapor-deposited silicon oxide, and evaporated silicon monoxide, were used to protect active and passive devices such as thin-film transistors[7] and sputtered NiCr resistors.[8] Figure 3 shows details of APL sputtered Cr and NiCr thin-film resistors with silicon monoxide passivation.

Today, APL can produce a variety of inorganic device passivations and encapsulants, including thermally grown silicon dioxide and plasma-enhanced deposition of both silicon dioxide and silicon nitride. Figure 4 presents typical deposition data for the films, and Table 1 presents basic properties of modern silicon dioxide and silicon nitride layers. The highlighted regions of Table 1 represent the processes currently practiced at APL. Table 2 summarizes the full range of chemical vapor deposition[9]

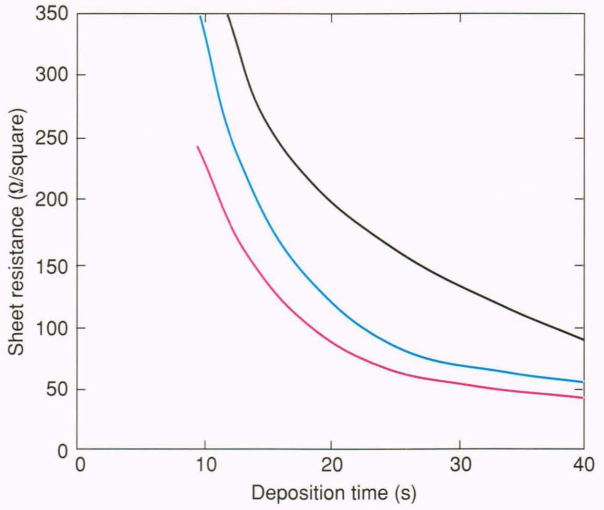

Figure 3. The change in sheet resistance with deposition time for sputtered chromium and nickel–chromium films. Black curve: Ni/Cr 50/50, Corning 0211 glass substrate, V_{RF} = 1.5 kV. Blue curve: Cr, AlSi Mag 772 ceramic substrate, V_{RF} = 1.0 kV. Red curve: Cr, 0211 glass substrate, V_{RF} = 1.0 kV. V_{RF} is the applied radio frequency sputtering potential. Sheet resistance is the electrical resistance of a material with the dimensions of a unit square and unspecified thickness.

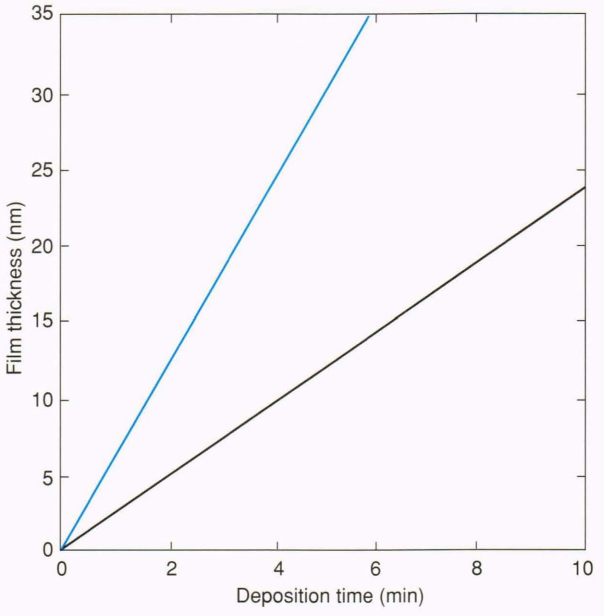

Figure 4. Increase in film thickness with time for the deposition of silicon nitride (Si_xN_y) (black curve) and silicon oxynitride (SiO_xN_y) (blue curve).

and plasma-enhanced[10] reactions possible with modern deposition science. Again, the highlighted regions illustrate the processes available at APL.

The Laboratory has also had experience with a large number of organic device passivations and encapsulants, including polyimide, epoxies, Parylene, urethanes, acrylics, and silicones. The basic properties of these materials are given in Table 3. The highlighted regions focus on the properties of Parylene and polyimide, two of the impor-

Table 1. Properties of inorganic passivations.

Property	Silicon dioxide					Silicon nitride	
	Thermal	Plasma	SiH_4+O_2	TEOS	$SiCl_2+N_2O$	LPCVD	PECVD
Deposition temperature (°C)	800–1200	200–350	400–450	650–750	850–900	650–750	200–350
Density (g/cm^3)	2.3	2.3	2.1	2.2	2.2	2.8–3.1	2.5–2.8
Refractive index	1.46	1.47	1.44	1.46	1.46	2.0–2.1	2.0–2.1
Relative dielectric constant	3.8–3.9	—	—	—	—	—	—
Dielectric strength (V/μm)	0.5–1.0	0.3–0.6	0.8	1.0	1.0	1.0	0.6
Room-temperature compressive stress (MPa)	200–400	300[a]	300[b]	100	300	1000[b]	200[c]
Coefficient of thermal expansion (10^{-6}/K)	0.5	0.64–1.1	0.64	0.64	0.64	4	4–7
Bulk resistivity (Ω·cm)	10^{14}–10^{16}	—	—	—	—	10^{15}–10^{17}	10^{15}

Note: TEOS = tetraethylorthosilane + O_2; LPCVD = low-pressure chemical vapor deposition; PECVD = plasma-enhanced chemical vapor deposition. Dashes indicate that data are strongly dependent on deposition conditions.
[a]Value of tensile stress is also 300 MPa at 25°C.
[b]Value represents tensile rather than compressive stress.
[c]Value of tensile stress is 500 MPa at 25°C.

Table 2. Chemical reactions for the formation of silicon dioxide, silicon nitride, and silicon films.

Material	Reaction	Temperature (°C)
Silicon dioxide	$SiH_4 + CO_2 + H_2$	850–950
	$SiCl_2H_2 + N_2O$	850–900
	$SiH_4 + N_2O$	750–850
	$SiH_4 + NO$	650–750
	$Si(OC_2H_5)_4$	650–750
	$SiH_4 + O_2$	400–450
	$SiH_4 + N_2O$	250–350[a]
Silicon nitride	$SiH_4 + NH_3$	700–900[b]
	$SiCl_2H_2 + NH_3$	650–750[c]
	$SiH_4 + NH_3$	200–350[a]
	$SiH_4 + H_2$	200–350[a]
	$SiH_4 + N_2O$	200–350[a]
	$SiH_4 + N_2O + NH_3$	200–350[a,d]
Silicon	SiH_4	600–650

[a]Plasma reactor.
[b]Atmospheric pressure.
[c]Reduced pressure.
[d]Silicon oxynitride.

tant coatings used at APL. Parylene is produced by the thermal dissociation of the dimer (di-*p*-xylylene) into a monomer (*p*-xylylene). Although the monomer is stable as a gas at low pressure, it spontaneously polymerizes upon condensation to produce a coating of high-molecular-weight, linear poly(*p*-xylylene), which is deposited at room temperature.[10]

The room-temperature deposition makes the Parylene process an attractive encapsulation process for all electronics. The deposit (nominally 25 to 50 μm thick) is an excellent conformal coating with superior step coverage and extremely low deposition stress. Films have excellent chemical resistance, with no incorporated impurities (especially in the nonchlorinated form) and no solvents. The Parylene coating is scratch-resistant and tough, and, because it is vapor deposited, it is suitable for coating hard-to-reach areas on, around, and under parts such as chips and beam leads.

Three substituted dimers and their resultant Parylenes are commercially available. Parylene N is an unsubstituted C-16 hydrocarbon, [2,2]-*para*-cyclophane(II); Parylene C is an aromatic chlorination of the dimer with one chlorine atom per aromatic ring; and Parylene D is an aromatic chlorination of the dimer with two chlorine atoms per aromatic ring. Properties of Parylenes N, C, and D are given in Table 4.

Parylene C has been used at APL to coat monolithic notch filters operating at C-band. The C-band notch filter uses an etched loop inductor (~3 nH inductance) and an etched interdigital capacitor (~500 fF capacitance) in parallel to form a null network at about 4.2 GHz on a 625-μm-thick copper-clad (copper thickness of 35.6 μm) Duroid circuit board with a relative dielectric constant of 10.8. A layout of the notch filter is shown in Figure 5. Figure 6 presents a typical curve of insertion loss versus frequency response for the filter with and without Parylene C (~15 μm thick). As Figure 6 shows, the change in performance was small. All other performance parameters changed less than 5%. Thus, Parylene C affords excellent circuit protection and reliability with little

Table 3. Properties of organic device and circuit passivations and coatings.

Properties	Parylenes	Polyimide	Polyurethanes	Silicones	Acrylics	Epoxies
Glass transition temperature (°C)	290–420[a]	>300	-70–130[b]	-55–150[b]	—	140–170
Dielectric constant at 100 Hz	2.6–3.0[c]	2.9–4.2[c]	3.5[d]	2.5–3.0	2.0	3.2
Dissipation factor at 100 Hz	0.0006–0.013[a]	0.002–0.006	0.03–0.04	0.0016–0.002	0.01	0.02–0.03
Dielectric strength (kV/mm)	185–275	>240	14–35	20–45	15–40	20–35
Volume resistivity (Ω·cm)	10^{16}–10^{17}	>10^{16}	10^{12}–10^{15}	10^{14}–10^{16}	10^{13}–10^{14}	10^{14}
Moisture absorption (%)	<0.1	0.5–3.5	0.4–0.65	—	—	1–6
Tensile strength (MPa) at 25°C	45–75	103–343	300–400	1.7–6.2	—	22–85

Note: Dashes indicate data not available.
[a]Melting point.
[b]Useful temperature range.
[c]At 1 MHz.
[d]At 10 GHz.

Table 4. Properties of parylenes N, C, and D.

Property	Parylene types N	C	D
Density (g/cm^3)	1.11	1.29	1.42
Refractive index	1.661	1.639	1.669
Melting point (°C)	420	290	380
Coefficient of thermal expansion at 25°C (10^{-6}/K)	69	35	—
Thermal conductivity (W/m·K)	0.12	0.082	—
Dielectric constant at 1 MHz	2.65	2.95	2.80
Dissipation factor at 1 MHz	0.0006	0.013	0.002
Dielectric strength (MV/m)[a]	275	220	215
Volume resistivity at 28°C, 50% RH (Ω·cm)	1.4×10^{17}	8.8×10^{16}	2×10^{16}
Moisture absorption (%)	<0.1	<0.1	<0.1
Tensile strength (MPa)	45	70	75
Yield strength (MPa)	42	55	60
Yield elongation (%)	2.5	2.9	3.0
Elongation at break (%)	30	200	10

Note: Dashes indicate data not available.
[a]Measured on 25-μm-thick film.

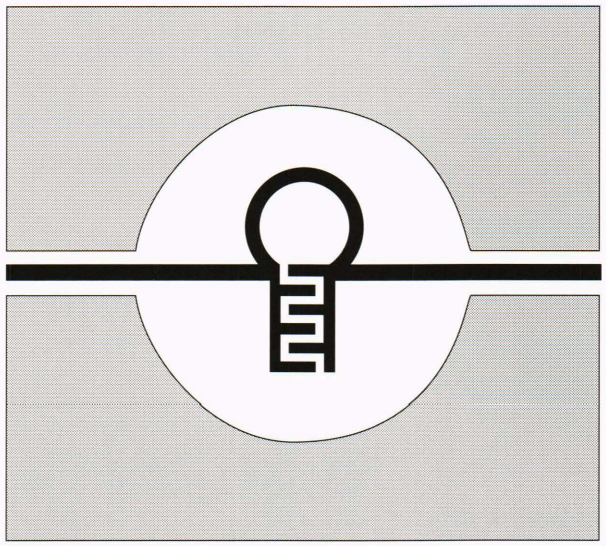

Figure 5. Layout of an APL-developed notch filter operating at 4.175 GHz. The notch filter is formed on 0.625-mm-thick Duroid circuit board ($\epsilon_r = 10.8$) with a copper track metallization thickness of 35.6 μm.

or no effect on performance. Note, in particular, Parylene's resistance to moisture absorption (Table 4).

Polyimide has also been used for device passivation and protection. The Laboratory has had extensive experience in using polyimide both as a device encapsulant and as an inner-layer dielectric. It is suitable for performance at high temperatures (>150°C), but requires curing at temperatures between 300 and 400°C for times in excess of thirty minutes. Both polyimides and acrylics exist in solid-sheet form and can be laminated on flat boards using pressure-sensitive acrylic and silicon adhesives, which are available in various thicknesses. Silicones cost more than acrylics but can be used at high temperatures. Solid films are shaped by punching or die cutting. Properties of various coating materials are listed in Table 3. Aspects of the use of polyimide and the details of polyimide chemistry will be described in the section on multichip modules.

Urethanes in the form of Solithane (Resin 113, Thiokol Chemical Corp.) and related resins have been used as printed wiring board (PWB) passivation and will be de-

scribed in the section on encapsulants and overcoats. The Laboratory has been particularly successful in using Solithane for board overcoating. Typical urethane properties are shown in Table 5. Urethanes or polyurethanes are available in one- or two-part systems that are solvent-based to achieve low viscosity for dipping, spraying, brushing, and so on. They are formed by reacting an isocyanate (R_1-NCO) with a hydroxyl (R_2-OH) compound to form a urethane group. Urethanes can be cured by heat or with internal catalysts. In thermally cured systems, the reactive isocyanates are inhibited by a readily volatilized or easily decomposed compound until the system is heated. In catalytically cured systems, the part containing the isocyanide is mixed with a second part containing the catalyst. In some systems, additional cross-linking is achieved by reacting amines or hydroxyl groups with the isocyanide groups. Because the isocyanates are highly reactive with moisture, moisture must be avoided before use.

The advantages of polyurethanes are good adhesion, rapid cure, good flexibility at low temperatures, excellent chemical resistance, low dielectric constant, and good moisture resistance.

SUBSTRATES

The substrates for most thick-film and thin-film circuits, except perhaps for silicon and gallium arsenide (GaAs) hybrid and multichip modules where active and passive elements can be built as an integral part of the substrate structure,[11] act as inert carriers for the conductors, passive components, and add-on active devices. In addition to the multichip-module-type constructs with active circuits built into substrates, as shown in Figure 7 and discussed later, the only other active role that a substrate has is in high-frequency or microwave applications, where it is an integral part of the electrical circuit. The substrate, however, does play a vital role in determining the properties of thin-film conductive and dielectric layers, as well as in determining much of the adhesion strength and reliability of printed thick-film layers. The substrate also contributes significantly to the cost of film circuitry because of surface finish, purity, and other material property requirements.

Commonly used substrates include glass, alumina, beryllia, aluminum nitride, silicon carbide, sapphire, quartz, silicon GaAs, spinels, and other ceramics. Alumina is probably the most common substrate material because of its excellent physical properties, resistance to chemical attack, high compressive strength, and relatively low cost. Table 6 compares alumina (99.6% purity) with other substrate materials used at APL. Typical thermal conductivities and coefficients of thermal expansion for common substrate materials are shown in Figures 8 and 9, respectively.

The Laboratory has developed a simple longitudinal bar apparatus[12] for measuring thermal conductivities of substrates with high thermal conductivity. The data points on the graphs in Figure 8 represent data produced by the APL apparatus. The data agree quite favorably with the manufacturer-supplied data. Measurement of the thermal

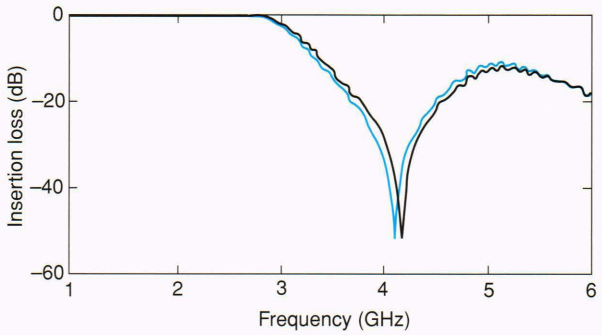

Figure 6. Insertion loss versus frequency plots for the APL 4.175-GHz notch filter. Before Parylene coat, black curve; after Parylene coat, blue curve.

Table 5. Properties of urethanes or polyurethanes.

Property	Value
Heat distortion temperature (°C)	10–65
Safe use temperature (°C)	90–130
Dielectric constant, 100 Hz–10 GHz	5–3.5
Dissipation factor, 100 Hz–10 GHz	0.016–0.04
Volume resistivity (Ω·cm)	10^{12}–10^{15}
Coefficient of thermal expansion (10^{-6}/K)	200–300
Moisture absorption (%)	0.4–0.65
Thermal conductivity (W/m·K)	5×10^{-5}
Dielectric strength (kV/mm)	14–35
Hardness, Shore A	40–70

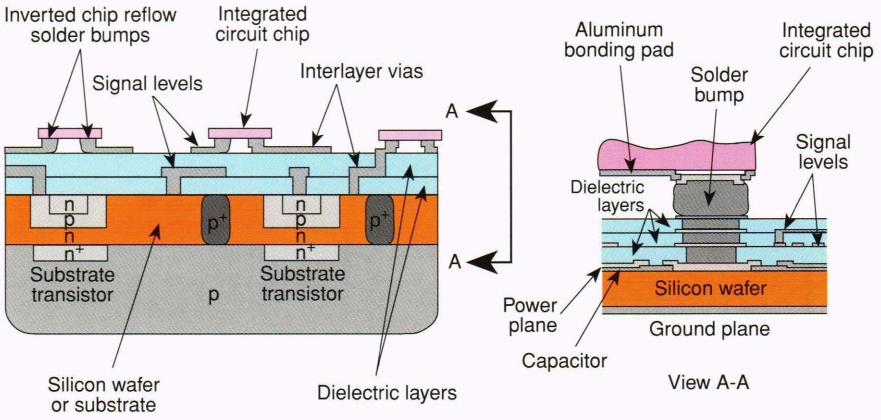

Figure 7. Cross section of a silicon-on-silicon hybrid as proposed by IBM in 1972 (see Ref. 12). View A-A shows details of the chip interconnect and interlayer via structure as envisioned by AT&T in 1987 (see Ref. 28). The terms n, p, n^+, and p^+ refer to semiconductor conductivity types; the plus (+) signs mean heavily doped.

Table 6. Properties of substrate materials used in microcircuit applications at APL.

Property	Al_2O_3 Thick film	Al_2O_3 Thin film	BeO Thin-thick film	AlN Thin film	AlN Thick film	AlN Thick film	SiC Thick film
Purity (%)	96	99.6	99.5	—	98	99.5+	—
Manufacturer	Coors	MRC	Brush–Wellman	Norton	Heraus	Tokuyama Soda	Hitachi
Color	White	White	White	Translucent (gray)	Gray	Translucent (gray)	Gray (dark)
Major impurity	Mg	Mg	Si	Y	Y	Ca	Be
Surface finish (μm)	<0.6	<0.096	<0.36	—	0.4–0.6	0.4–0.6	—
Average surface roughness (μm)	0.49	0.14	0.16–0.33	0.32	0.77	0.88	0.17
Grain size (μm)	—	<1.5	9–16	—	5–10	—	—
Average grain diameter (μm)	9	1	16	Polished	13	17	Machine surface
Thermal conductivity (W/m·k)	26	37	250	170	140–170	140	270
Coefficient of thermal expansion (10^{-6}/K)	7.1	7.1	9.0	4.6	4.2	4.4	3.7
Dielectric constant at 1 MHz	9.5	9.9	6.5	8.8	10	8.9	40
Dissipation factor at 1 MHz	0.0004	0.0001	0.0004	0.0005	0.002	0.001	0.05
Resistivity at 25°C (Ω·cm)	$>10^{14}$	$>10^{14}$	10^{15}	$>10^{14}$	$>10^{14}$	10^{13}	$>10^{13}$
Hardness, Rockwell 15N	95.5	96.3	90.9	94.0	94.5	93.8	99.0
Flexural strength (MPa)	400	620	241	392	280–320	441[a]	450

Note: Dashes indicate data not available.
[a]Bending strength.

conductivity of actual substrate lots is vital to accurate thermal design. Variations in thermal conductivity from lot to lot, even for substrates supplied from the same manufacturer, can be as high as 20%. For one mismarked lot of aluminum nitride material, the thermal conductivity was given as 140 W/m·K but was measured to be less than 70 W/m·K.[12]

Although alumina is the workhorse of the electronic hybrid and packaging industry, aluminum nitride exhibits very attractive properties. Especially attractive are its higher thermal conductivity and its close match in coefficient of thermal expansion to both silicon and GaAs.

Before film deposition or formation of the film circuit elements and conductors, the substrates must be cleaned. Standard cleaning cycles use hydrocarbon solvents or immersion in fluorocarbon liquids or vapors. Cleaning with hydrocarbon solvents has not been particularly successful,[13] whereas cleaning with fluorocarbons, although effective, now faces serious restraints because of the effects of fluorocarbons on ozone layer decomposition. In addition to furnace firing,[14] high-temperature baking, and the vacuum outgassing of thin-film substrates, ultraviolet (UV)/ozone exposure[15,16] has been shown to be a particularly effective cleaning process. In fact, APL researchers[16] have shown that UV/ozone exposure can reduce contact angles (when compared with solvent cleaning alone) on all the substrates listed in Table 6.

METALLIZATIONS

Metallizations for electronic packaging applications fall into three primary categories:

1. Pure elemental or compound materials deposited over the full substrate areas by various vacuum material decomposition and plating techniques and then patterned by photolithography (i.e., thin films).
2. Mixtures of various materials (filler, binder, and solvent) forced through patterned screens or stencils onto substrates and then dried and fired to affix the film layer (i.e., thick films).
3. Metal foil sheets or layers laminated (glued) to various reinforced organic layers (i.e., PWB's). The laminated foil layer technology will be described in the section on circuit boards.

Fabrication of thin-film metallization begins by deposition of a materials layer on a selected substrate. The choice of substrate and its influence on film properties

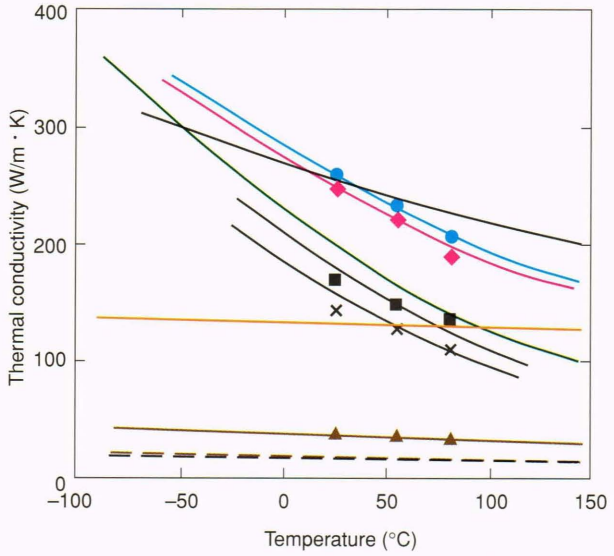

Figure 8. Thermal conductivities for typical substrate materials. The data points represent measurements performed at APL using the APL longitudinal bar apparatus (see Ref. 13). Aluminum nitride (solid black curves), silicon carbide (blue), beryllia (red), silicon (green), molybdenum (orange), 99.6% alumina (solid brown), 92% alumina (dashed brown), and Kovar (dashed black).

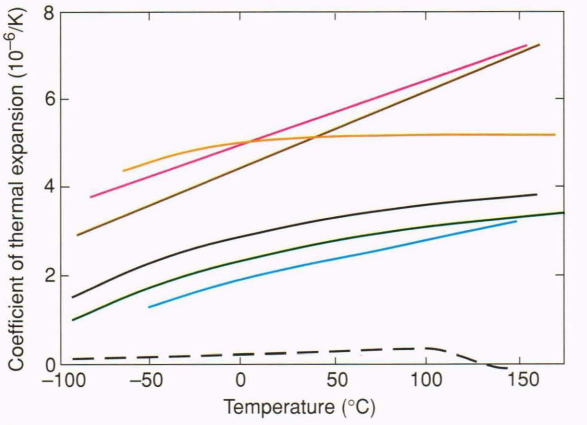

Figure 9. Coefficients of thermal expansion for typical substrate materials. Aluminum nitride (solid black curve), silicon carbide (blue), beryllia (red), silicon (green), molybdenum (orange), alumina (brown), and epoxy-graphite and epoxy-kevlar (dashed black).

will be discussed later in this section. Thin films have been deposited on substrates by numerous methods,[16] including sputtering, vacuum evaporation, chemical vapor deposition, plating, anodization, and pyrolysis. Sputtering and, to some extent, vacuum evaporation are the mainstays of the industry. In sputtering, a bombarding plasma ion source is created, the ions are directed onto a target (of the material to be deposited), and the target atoms driven off by the force of the ion collisions are subsequently collected (on a substrate). Current emphasis is on magnetron sputtering, which applies a high magnetic field in the vicinity of the target (cathode) to increase the plasma density and, hence, the sputtering rate.

The electrical properties of thin metal films may differ significantly from those of bulk material. Film properties are influenced by deposition technique (e.g., evaporation or sputtering), purity of source material, substrate material, substrate cleaning (and outgassing), substrate temperature, deposition rate, angle of incidence of the impinging film with respect to the substrate, and ambient atmosphere within the chamber.

Aluminum, gold, and copper (with appropriate adhesion layers such as chromium, tantalum, or titanium) have historically been the most common thin-film conductor materials. Thin-film resistors[8] have been fabricated from many alloys and components; nickel chromium (NiCr) and tantalum nitride (TaN or Ta_2N) compositions are the industry standards. Inorganic dielectrics of silicon dioxide (and monoxide) and silicon nitride have been used as insulating films for many years to passivate resistors and fabricate capacitors. Figure 10 shows a high-frequency monolithic capacitor fabricated at APL using a silicon substrate with Si_3N_4 as the dielectric material and chromium/gold as the metallization. Today, newer organic insulators such as polyimide are being used to fabricate thin-film multilayer conductor structures.

Copper is the most widely used conductor material for multilayer applications, for several reasons: its high electrical conductivity; its solderability, which permits both flip-chip and solder-reflow-type tape automated bonding assembly; and its ability to be electroplated with relative ease to thicknesses greater than 5 μm, thus making an extremely low resistance interconnect even for metallization lines as narrow as 1 μm.

Copper can be gold flashed for surface layer applications involving gold or aluminum wire bonding; similarly, all-gold surface metallizations have also been used.

Copper must be used with an adhesion layer because it has poor adhesion to polyimide (or to the ceramic host substrate). Because copper metallization is prone to corrosion owing to the high moisture absorption (~1%) by the polyimide, a passivation layer must be sputtered or plated over the copper to help resist corrosion. For low-speed, low-density applications where traces can be 50 μm wide or larger, the adhesion layer, the copper conductor, and the passivation layer can be sequentially deposited onto the substrate. When signal traces are narrow, line resistance is reduced by electroplating additional copper to increase the metallization thickness. Figure 11A outlines typical metallization patterning techniques for both inner conductor layers and surface conductor layers used in typical multilayer thin-film schemes with polyimide dielectrics. Figure 11B shows a typical APL multilayer test vehicle using these metallization methods.

Aluminum has been used in multilayer structures with polyimide, but it is more resistive than copper and has reliability problems in nonhermetic applications.[17]

DIE ATTACHMENT AND INTERCONNECT

The electrical connection to most integrated circuits is made to bonding pads on the surface or the face of the chip. To provide mechanical support (and sometimes a back surface electrical or thermal interconnect), the chip or integrated circuit is bonded to the substrate or package using eutectic die attach, metal alloy (solder) attach, or organic adhesive attach.

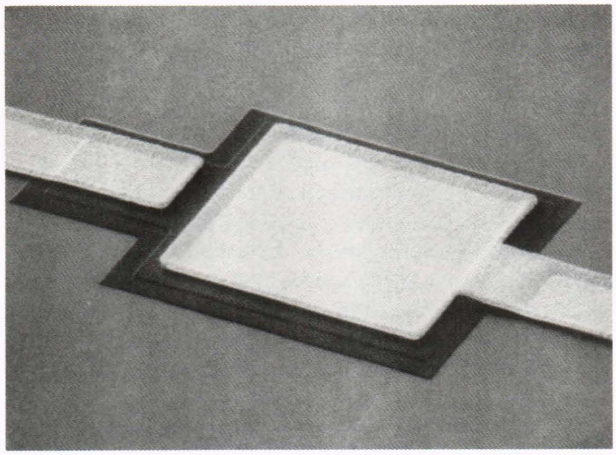

Figure 10. APL monolithic microwave capacitor.

The eutectic die attach typically used is the gold–silicon eutectic (94 wt.% gold, 6 wt.% silicon), which melts at 370°C. The gold–silicon eutectic bond can be formed in several ways. The simplest method is to place a silicon die into intimate contact with a gold-plated surface and then raise the temperature above 370°C. A simple "scrubbing" motion helps the bond to form, as does a gold metallization on the back of the chip. Another technique, preferred by several manufacturers, is the use of a thin sheet of the eutectic alloy (a preform) between the chip and the substrate (or package) metallization. Regardless of the technique, it is essential that sufficient gold be present to ensure that the alloy forms properly.[18]

Other metal alloys with either unique melting points or practical solidus–liquidus ranges have been used for die attach (Table 7). Because they do not rely on the interdiffusion of gold with silicon (and the formation of the gold–silicon eutectic), either a thin sheet of the alloy or pretinning (for tin–lead solders) must be used between the metallized back of the chip and the metallized region of the substrate or package bottom. Alloy die bonds provide good mechanical strength and electrical conductivity, and low thermal impedance. Some alloys or solders require flux to aid in the reflow and prevent excessive oxidation. If flux is used, it must be removed, thereby introducing extra processing, cleaning, and inspection steps.

The die can also be bonded to the package or substrate using organic adhesives such as epoxy, polyimide, and other thermoset or thermoplastic materials. Because organic adhesives typically have poor thermal and electrical conductivity, gold and silver are commonly introduced to improve those properties. Thermal performance can also be improved without sacrificing electrical isolation by introducing thermally conductive particles such as alumina or beryllia.

A perceived disadvantage of the organic adhesive bond is the potential for outgassing, or the subsequent release of adsorbed gas or moisture during periods of thermal stress. The outgas products (known and unknown contaminants) can adversely affect device reliability and, hence, product lifetime. The poor thermal stability of organic adhesives (especially above the glass transition

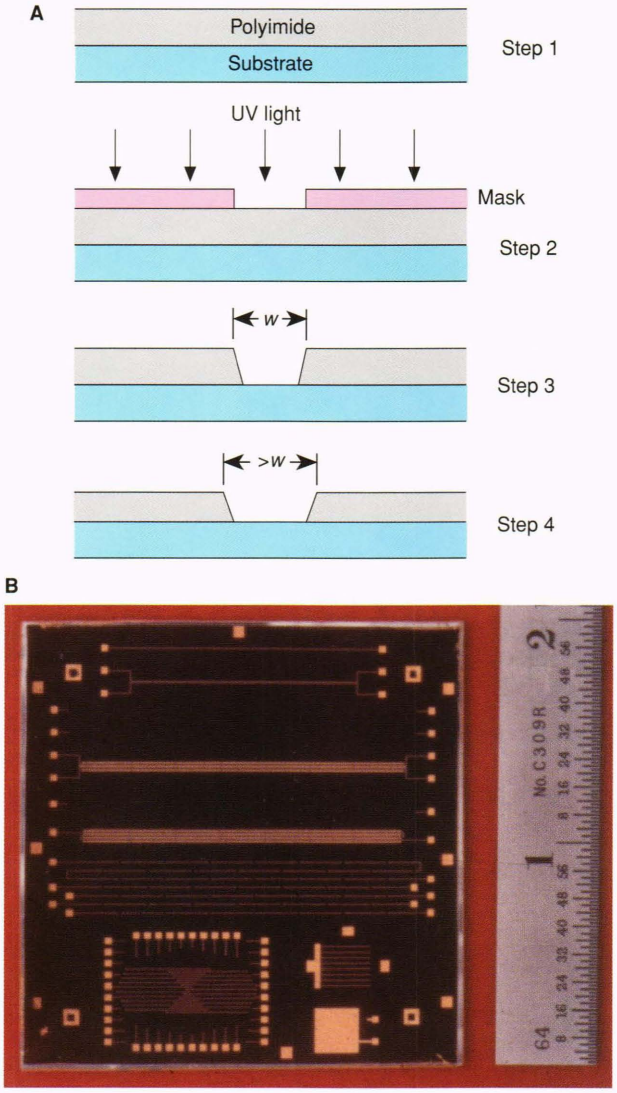

Figure 11. Patterning technique for a polyimide that can be photoimaged. **A.** Patterning sequence: (step 1) apply polyimide and soft bake at ~80°C, (step 2) expose through mask, (step 3) develop, and (step 4) cure at 380°C. **B.** Test structure.

temperature), coupled with the outgassing of trapped solvents and reaction by-products, has produced significant concerns for VLSI circuit die attach reliability.

Silver-filled glass materials with low melting points (≈400°C) have emerged as a bonding alternative for VLSI die attachment. The use of 400°C temperatures and oxidizing environments (necessary for achieving proper adhesion reactions) has caused major reliability concerns in processing. These materials also contain solvents and binders, giving rise to many of the outgassing problems associated with organic adhesives. The current die attach methods available at APL are shown in the highlighted portions of Table 7.

INTERCONNECTION

Integrated circuit electrical interconnection or bonding is accomplished in three primary ways: wire bonding, TAB, and inverted-chip reflow. In wire bonding, a metal

Table 7. Comparison of properties of various die attach alloys and typical organic adhesives.

Material	Composition, weight % [atomic %]	Melting point (°C)	Resistivity (10^{-6} Ω·cm)	Coefficient of thermal expansion (10^{-6}/K)	Thermal conductivity (W/m·K)
Die attach alloys					
Gold–silicon (eutectic)	Au(94)–Si(6) [Au(82)–Si(18)]	363	—	12.3	27
Gold–tin (eutectic)	Au(80)–Sn(20)	280	16	15.9	57
Tin–lead (eutectic)	Sn(63)–Pb(37) [Sn(74)–Pb(26)]	183	—	—	52
Tin–lead (eutectic)	Sn(5)–Pb(95)	310	19	29	36
Organic adhesives					
Epoxy (silver-filled)	10–50[a]	80–100[b]	—	53	0.08–0.8
Epoxy (unfilled)	Novolac[c]	80–100[b]	10^{14}–10^{16}[d]	60	0.02
Epoxy (AlN-filled)	10–50[a]	80–100[b]	10^{11}–10^{13}[d]	22	0.80–4.0

Note: Dashes indicate data not available.
[a]Filler percentage.
[b]Glass transition temperature.
[c]Novolac is a trade name for epoxy resins of di-glycidyl ethers of bisphenol A or bisphenol F.
[d]Volume resistivity in units of Ω·cm.

interconnect wire is placed in intimate contact with the chip bonding pad, the substrate, or the package pin. Under proper conditions of temperature, pressure, and perhaps ultrasonic energy, the metal wire and the underlying pad metallization are fused or welded to effect the electronic interconnection.

Wire bonding is divided into three primary categories, depending primarily on the mechanism used to create the weldment: thermocompression bonding (ball-wedge), thermosonic bonding (ball-wedge), and ultrasonic bonding (wedge-wedge). The Laboratory has been particularly active in thermosonic bonding (Fig. 12), which uses force and associated capillary and substrate heat along with ultrasonic energy to effect the bond. The ultrasonic energy is introduced by vibrating or resonating the wire capillary affixed to the end of an ultrasonic transducer horn.

The Laboratory has developed techniques for optimizing the thermosonic process.[19] Figure 13 shows the improvement in wire bond shear strength achieved by using the APL process rather than the setup recommendations of the bonding machine manufacturer. The Laboratory has been a pioneer in the use of the ball shear test[20] for thermosonic ball bond evaluations and bonding machine setup. The basic shearing process is illustrated in Figure 14. A comparison of test information obtained with the wire bond pull test and the ball shear test is summarized in Table 8. These methods are complementary; together they constitute a complete evaluation. The Laboratory performed the basic round-robin testing[21] necessary to validate the ball shear test as a Standard Test Method[22] for the American Society of Testing and Materials (ASTM). That test, ASTM Method F-89, is soon to be included in Military Standard 883C for microcircuit qualification. It has helped APL evaluate the gold-aluminum intermetallic system[23] used on chips and in hybrid structures, leading to more reliable wire bonds and further understanding of materials-related bonding phenomena such as cratering.[24]

The TAB process involves bonding integrated circuits to patterned metal on multilayer tape (i.e., a patterned copper foil layer on a polyimide carrier film) using thermocompression (heat and pressure) bonding techniques.[25] Once attached to the carrier film, the integrated circuit can be tested, placed in a package, encapsulated, and environmentally stressed before excisement from the tape and attachment to the board or substrate by outer lead bonding (typically soldering or alloy reflow). The TAB leads are planar beams. In multilayer tape structures with ground planes, TAB can provide controlled impedance interconnects.

The inverted-chip reflow process involves the formation of balls or bumps on the chip bonding pads (either solderable or nonsolderable bumps). Once bumps are formed, the chip is inverted over appropriate metallization pads on the substrate or package, and an interconnection is formed by solder reflow, thermocompression, or ultrasonic techniques. The Laboratory has developed a method for forming bumps on chips using a ball bonding technique. The inverted interconnect can have extremely high density, with excellent electrical performance[25] and great amenability to automation. The inverted nature hides the device's face, which causes concern regarding inspection but provides a free back for thermal control, for example.

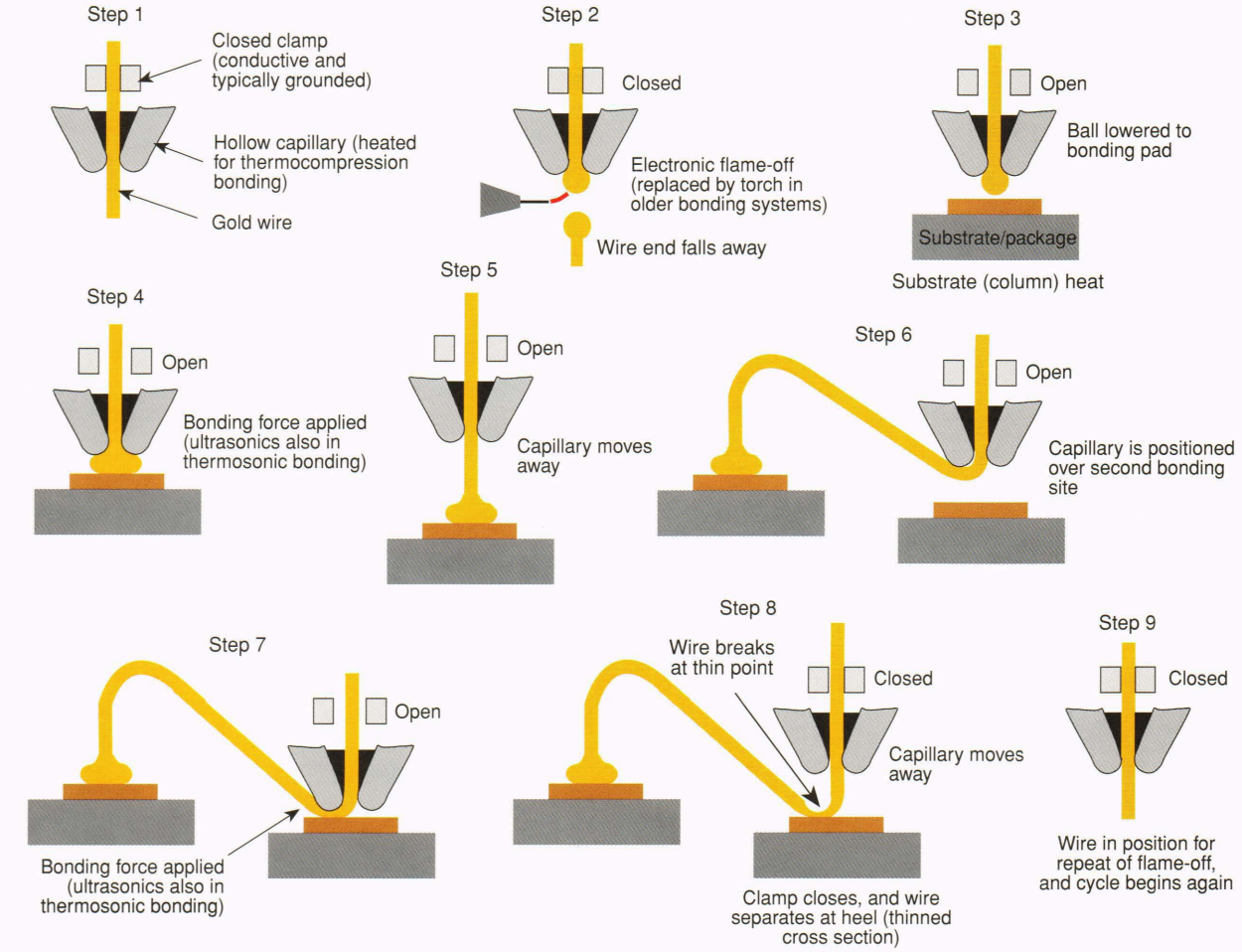

Figure 12. Steps in the ball-wedge bonding process (thermocompression or thermosonic bonding).

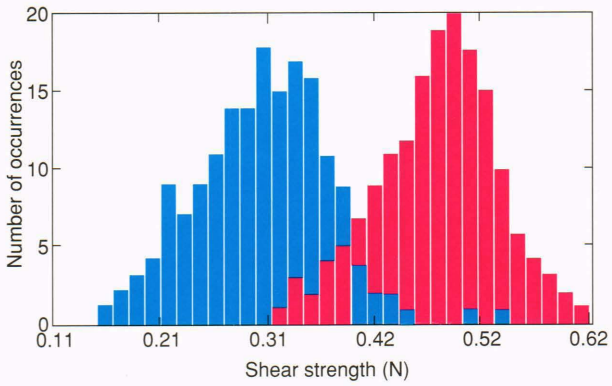

Figure 13. Gold ball bond shear strength for wires bonded to aluminum metallization (on silicon). The blue histogram shows the results from the bonding machine setup using the wire bond pull test as recommended by the machine's manufacturer (mean = 0.32 N, $\sigma = 0.039$ N, $n = 171$). The red histogram shows the results from optimization of the bonding process using the ball shear strength as the response parameter (mean = 0.46 N, $\sigma = 0.061$ N, $n = 169$).

BOARD-LEVEL PACKAGING

The structure and the process of joining packages to higher-level assemblies (e.g., cards, boards, or substrates) greatly influence electronic system design, manufacturability, cost, and reliability. The choice of board interconnection method also plays a primary role in determining board configuration and materials selection. The choice of interconnection method is influenced by the need for parts to be removable so that failed parts can be replaced, or a part can be changed to achieve enhanced performance.

These criteria usually lead to a solder joint (or sometimes a socket) that can produce a high-performance electrical interconnect with sufficient reliability (in properly designed structures) and an appropriate degree of impermanence to allow a device to be repaired. Basic forms of packages and soldered interconnects are shown in Figure 15. The major alternative to a solder joint for interconnecting the package to the board is a mechanical, pluggable (pin-socket) interconnection. The interconnection allows the package to be removed easily and is particularly suited for upgrade and repair in the field, as well as for initial module testing. Pin-socket interconnections typically do not perform as well as the more permanent solder joint. Other alternatives may include conductive adhesives or the direct chip-on-board type[26] with wire bonded interconnections, although repair when either of these is used may be extremely difficult.

The increasing density of integrated circuits has forced a significant increase in chip input/output (I/O) and a cor-

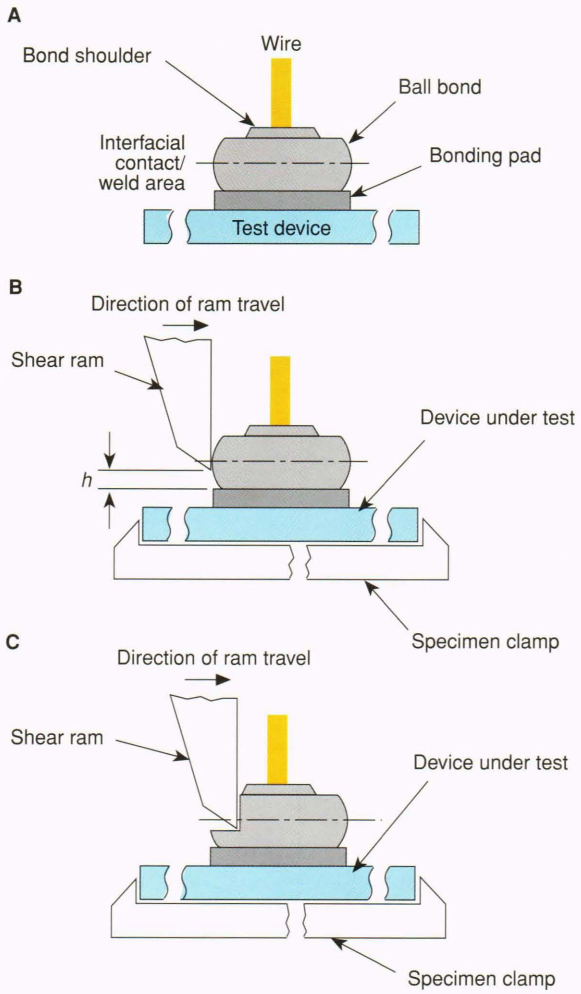

Figure 14. The ball bond shearing process. **A**. Basic bond. **B**. Ram in initial position (below the ball centerline but at least 25 μm [*h*] above the pad). **C**. Ram beginning the shearing operation.

responding increase in wiring density on the mating circuit boards. The need for increased density has forced the development of greater packaging and board density than could be achieved by the standard dual-in-line package (DIP) with its regular, wide lead-spacing (1.27- or 2.54-mm grid) column vias and through-hole mounting. The new packaging direction is surface (i.e., leadless) mounting on boards with staggered (blind) vias and no wasted area. The through-hole, mounted, pinned package now accounts for about 56% of the industrial and consumer electronic package markets, but this number is projected to drop to less than 50% by 1995 as the transition to automated surface-mount assembly continues worldwide.

THROUGH-HOLE MOUNTING

In through-hole mounting, the lead from the package is formed (shaped or bent, for an axially leaded device) and then pushed through a hole in the PWB (Fig. 15). The hole is typically plated, and the lead is soldered into the hole to effect both a mechanical and electrical interconnection. The mainstay through-hole package has been the DIP, which has been used for integrated circuit packaging

Table 8. Information that can be derived from wire-bond pull test and ball-bond shear test.

Information	Wire bond pull test ASTM F795	Ball bond shear test ASTM F795
Hybrid/bonding pad/package pad layout	Yes	No
Wire bond geometry	Yes	No
Wire quality (bondability, defects, etc.)	Yes	No[a]
Second bond	Yes[b]	No
Bonding machine/parameter optimization	No[c]	Yes
Process development (cleaning, metallization, etc.)	No[c]	Yes
Substrate/bonding pads	No[c]	Yes

[a]Sensitive to wire impurities; insensitive to mechanical defects.
[b]Extremely dependent on wire bond geometry.
[c]Insensitive unless the effect causes catastrophic first or second bond adhesion.

since the early 1960s. In the DIP, the high-density chip I/O is fanned out over a larger area to meet the wiring density of the PWB. A typical DIP-populated board fabricated at APL is shown in Figure 16. The DIP typically has leads on 2.54-mm centers along two opposing edges of the package. It can come with up to 64 leads, but the electrical performance of large DIP's is significantly poorer than that of equivalent-lead-count packages of the surface-mount type such as chip carriers or quad flat packages. The ratio of the length of the longest lead to the length of the shortest lead on a large DIP is about 7 to 1, whereas in an equivalent chip carrier, the same ratio is 1.5 to 1.

In a pin-type package, the primary alternative to the DIP is the pin grid array, in which the entire area of the package bottom is covered with pins. The pin grid array costs more but performs better than the DIP in all areas, especially in connections for a given package area (see Fig. 2).

Surface-mount technology (SMT) provides many alternatives to pinned packages and through-hole mounting. Reasons for using SMT include increasing density, reduced package size (and cost), improved board area utilization, better electrical performance, and improved repairability. Two principal types of surface-mount packages are used: leadless packages, which include leadless chip carriers, pad grid arrays, and certain fundamental surface-mount elements such as chip capacitors, resistors, and inductors; and leaded packages, which include chip carriers (J-lead), quad flat packages, gull wing packages, and butt-joint packages.

In the leadless packages, solder forms the bridge between the metallized areas of the package and the board. The solder's geometry and, hence, its performance[27] are determined by the package placement; solder volume; pad lengths; solder material; solder reflow processing during the joint operation; and mismatch in coefficient of thermal expansion of the package, board, and solder. In the leaded packages, a compliant lead extends from the

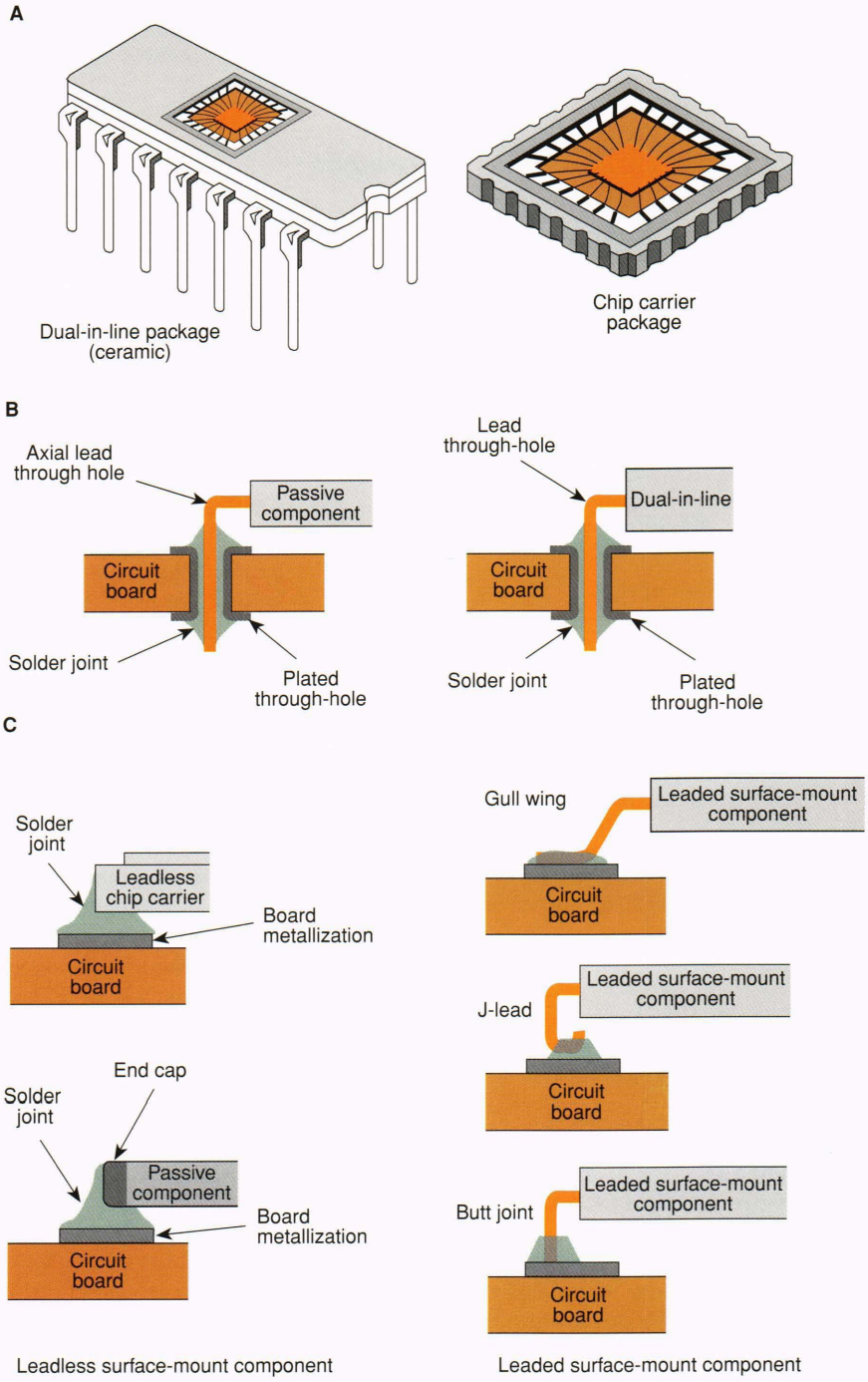

Figure 15. Package and package-mounting concepts. **A**. Common through-hole (dual-in-line) and surface mount (chip carrier) packages. **B**. Through-hole mounting. **C**. Various types of surface-mounting schemes.

package and forms the interconnection of the package by means of a solder joint to the board. This compliant lead reduces the stresses and strains in the solder joint by flexing under applied loads, thus improving reliability. For both the leadless and leaded packages, the solder joint forms both the electrical and mechanical connections between the board and the package. Surface-mount technology will continue to grow as automated assembly continues to increase. Through-hole mounting, however, will continue to be used. It is common to find both SMT and through-hole mounted components on the same board.

The major distinction between leaded and leadless SMT is the elastic compliance of the interconnecting lead in the leaded device between the package and the board. The elastic compliance becomes important under conditions of thermal and power cycling[28] of the package-board systems. Researchers at APL have performed many analyses[29] and experiments[30] to estimate the reliability performance (cycles to failure) of both configurations. Results have produced certain design rules for the design and fabrication of reliable solder joints,[30] but the process is far from complete. Solder joint reliability is the major concern in all surface-mount applications.[31]

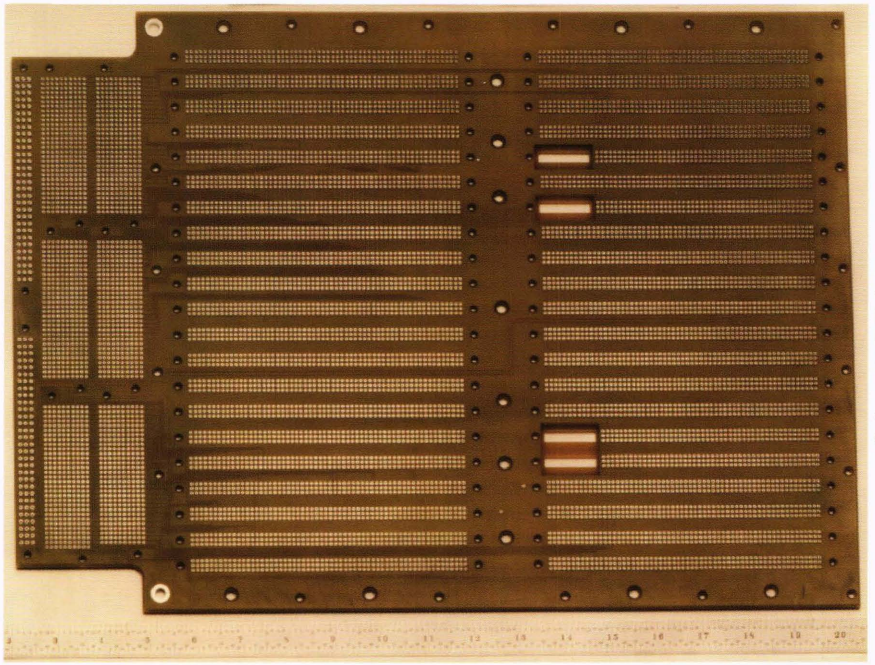

Figure 16. Example of a multilayer epoxy-glass printed wiring board fabricated in the recently certified Printed Wiring Board Facility of APL's Engineering and Fabrication Branch. The board is 13 in. × 18 in. and contains twenty-four layers (seventeen signal, five power/ground, and two external pad layers).

CIRCUIT BOARDS

A circuit board may be considered a composite of organic and inorganic materials with both internal and external wiring that allows components to be mounted (mechanically supported) and electronically interconnected. For the sake of this discussion, thin-film and thick-film inorganic circuit board or substrate constructs are excluded (these are described elsewhere[16,32]). Four basic printed board technologies are used: rigid boards, flexible boards, metal core boards, and injection-molded boards.

The materials used in the manufacture of printed boards (except metal core boards and injection-molded boards) are copper-clad laminates of organic dielectrics, which include phenolic paper, epoxy glass, polyimide glass, and others (to a lesser degree). Polyimide is being used increasingly because of its high-temperature stability and excellent handling properties. Epoxy-glass laminates (of the FR-4 type, which is a fire-retardant, epoxy-glass cloth)[33] are the most widely used printed board material. Polyimide glass is the second most important board technology. Properties of both of these laminates are given in the shaded portion of Table 9. The typical epoxy resin is the diglycidyl ether of 2,2-bis(4-hydroxyphenyl)propane, which is referred to as a bisphenol A (BPA) base system. Other resins and reinforcement used in printed boards are summarized in Table 9. The basic definitions used in the description of printed boards are shown in Figure 17.

Printed wiring boards range in complexity from single-sided to complex, multilayer boards that, in principle, can be any number of layers. For example, boards of forty to fifty layers have been demonstrated.[34] Typical cores (an insulation layer sandwiched between two patterned metal layers) are interleaved with insulation layers (epoxy-glass or polyimide-glass prepregs) to build the board structure to the designed thickness, and then the whole sandwich is laminated. Drilling and plating connect the layers vertically with plated through-holes. Buried vias can occur when the two circuit layers of a core are interconnected by a plated via (through-hole) before lamination. Details of printed board fabrication have been described by Tummala and Rymaszewski.[35]

The Laboratory has been building multilayer PWB's for some time using both epoxy and polyimide board materials. The Laboratory's PWB facility, housed in the Steven Muller Center for Advanced Technology, has been described in an article by Feldmesser et al.[36] The facility is currently certified to MIL STD 55110-P[37] for the fabrication of both multilayer epoxy-glass and polyimide-glass boards.

MULTICHIP MODULES

The progress of microelectronics toward more complex and faster device technologies has resulted in a revolution in packaging. Today's packaging technologies must accommodate the high I/O capabilities, as well as the increased operational speed, of today's VLSI devices. The PWB's and thick-film hybrids of yesterday are no longer adequate to meet the extremely dense wiring requirements of the state-of-the-art silicon devices. Multilayer multichip module structures with line geometries of 25 μm (on 99.6% Al_2O_3) or less (on silicon or sapphire) are required to meet the packaging and interconnection challenges of tomorrow. A summary of multichip module types is given in Table 10.

The thin-film multichip module structure typically consists of alternate layers of patterned metal conductors and insulating dielectric materials deposited on a host substrate that provides the mechanical support for the multilayer circuitry. Ideally, the metal conductor should possess a high electrical conductivity to accommodate

Table 9. Properties of printed wiring board laminates and polymer resins.

Material	Glass transition temperature (°C)	Dielectric constant at 1 MHz	Dissipation factor at 1 MHz	Volume resistivity (Ω·cm)	Coefficient of thermal expansion (10^{-6}/K)[a]	Moisture absorption (%)
Laminates[b]						
Epoxy-fiberglass	120–130	4.0–5.5	0.02–0.03	10^{12}	14–20 (*x*,*y*) 50–70 (*z*)	0.1–0.3
Polyimide-fiberglass	210–220	4.0–5.0	0.01–0.015	10^{14}	12–16 (*x*,*y*) 40 (*z*)	0.15–0.4
Epoxy-quartz	125	—	—	—	6–12 (*x*,*y*)	—
Polyimide–quartz	250	3.4	0.005	—	6–12 (*x*,*y*) 34 (*z*)	—
PTFE[c]-fiberglass	75	2.3–2.5	0.0008–0.02	10^{10}	20	1.10
Epoxy-kevlar	—	—	—	—	6–10 (*x*,*y*) 90(*z*)	—
Polyimide-kevlar	—	3.6	0.008	—	3–7 (*x*,*y*) 84 (*z*)	—
Epoxy-aramid	125	3.9	—	10^{16}	6–8 (*x*,*y*)	0.85
Polyimide-aramid	250	4.0	—	10^{12}	5–8 (*x*,*y*)	1.5
Resins						
Epoxy (Novolac)	140–170	3.2	0.016	10^{14}–10^{16}	—	1–6
Polyimide	>300	2.9–4.2	0.002–0.006	10^{16}	3–50 (*x*,*y*) 3–45 (*z*)	0.5–3.5
PTFE[c]	19[d]	2.1–2.8	0.0004	—	65 (*x*,*y*) 84 (*z*)	—
Polyacrylate	—	3.0–3.8	—	—	62–63 (*x*,*y*)	—
PEEK[e]	143	3.0	—	—	40 (*x*,*y*)	—
PBZT[f]	250	3.0	—	—	9 (*x*,*y*) 20 (*z*)	—
Benzocylobutene	250–350	2.6–2.7	0.0004–0.003	—	35–66 (*x*,*y*)	0.02

Note: Dashes indicate data not available.
[a]*x*,*y* are in-plane axes; *z* is normal axis.
[b]Resin plus reinforcing fiber (resin-fiber).
[c]PTFE = polytetrafluoroethylene.
[d]Crystal phase change triclinic-trigonal.
[e]PEEK = polyether ketone.
[f]PBZT = poly(*p*-phenylene benzobisthiazole).

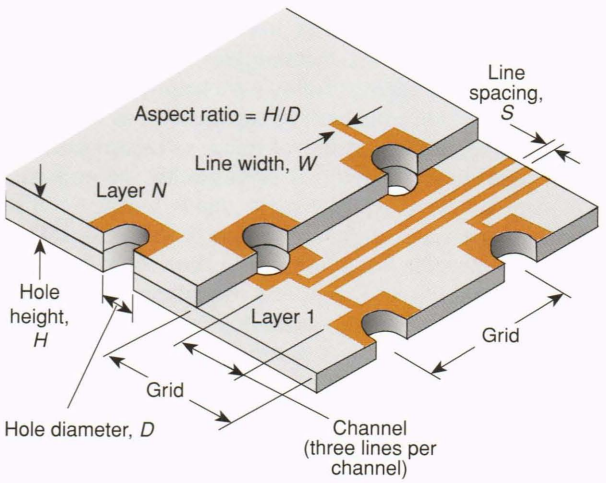

Figure 17. A board cross section, illustrating layer stacking and critical dimensions. Wiring capability = (lines per channel × layers)/grid.

the reduced line widths required for high-density applications. Typically, thin-film copper is used in combination with other thin-film layers that offer good adhesion characteristics and can provide corrosion resistance. The dielectric material should possess a relatively low dielectric constant to minimize interdevice signal delays, while permitting the fabrication of characteristic impedances within the 50- to 90-Ω range. The dielectric material should also be compatible with existing thin-film processing methods and offer the good planarizing or leveling characteristics necessary for fine-line multilevel structures. Polyimide has traditionally been used as an interlayer dielectric, although newer dielectric materials have recently been used that tend to have a lower percentage of moisture absorption.[16]

The multichip module concept is a packaging scheme that has become attractive with the development of the multilayer thin-film hybrid structure. This scheme uses to advantage the increased line density that the thin-film multilayer hybrid has to offer, permitting the direct

Table 10. Multichip module (MCM) parameters.

	MCM-C		MCM-D		MCM-L
Parameters	Cofired ceramic	Low-K ceramic	Silicon on silicon	Low-K (organic dielectrics on ceramic, metal, etc.)	Printed wiring boards
Line Density (cm/cm^2)	20	40	400	200	30
Lines/spaces (μm)	125/ (125–375)	125/ (125–375)	10/ (10–30)	(15–25)/ (35–75)	750
Dielectric constant	9	5	3.6–4.0	2.4–4.0	3.5–5.0
Input/output ($\times$ 1000)	1.6–6.4	1.6–6.4	0.8–3.2	0.8–3.2	1.6–3.2
Substrate area (cm^2)	225	225	100	100	500+
Terminating resistors	Built-in	Built-in	Built-in	Surface mount	Surface mount
Decoupling capacitance	Surface mount	Surface mount	Built-in	Built-in or surface mount	Surface mount
Transmission lines	Stripline μstrip	Stripline μstrip	Stripline μstrip, 50 Ω	Stripline μstrip, 50 Ω	Stripline μstrip

Note: μstrip denotes microstrip.

mounting and routing of multiple VLSI and very-high-speed integrated circuit chips on a single small substrate that can be then be mounted in a hermetic package or simply coated with a moisture-resistant encapsulant. The multichip module (multichip hybrid) usually represents a partitioned element in a larger electronic system such as a bank of random access memory or a special-purpose processing unit. Because of the high degree of functionality of the partitioned logic, the number of external leads can be significantly higher than what would be predicted, by the number of internal logic gates, using a typical Rent's Rule calculation.[38]

Rent's basic concepts for single-chip packages have been extended to multichip modules by Charles and Clatterbaugh[39] of APL with excellent predictive results for high-density packaging. The increased package outline for the multichip module compared with that of standard single-chip packages offers the circumference needed for the high lead counts (or larger area for area array-type modules). The higher density can improve system power distribution by allowing the use of multiple chips instead of a single high-heat-dissipating one without a significant signal delay penalty. The module can also accommodate special heat sink options that may not be as readily adaptable to smaller units. Finally, the manufacture of multichip modules may result in significant cost savings. Although the costs involved in fabricating these complex modules may be high initially, at least one estimate predicts that for almost every level of interconnection density, the cost of packaging bare chips onto an intermediate package and interconnecting it to a simpler PWB is cheaper than interconnecting individually packaged chips on a more complex PWB.[40]

Polyimide is the most widely used material for multilayered thin-film module structures because of its low dielectric constant ($\epsilon_r = 3.5$), solvent resistance, high glass transition temperature (T_g), and excellent planarization characteristics. The resistance to attack by solvents makes polyimide suitable for use with wet chemical etching of thin metal films. Its high-temperature stability ($T_g = 280°C$) makes it ideal for metallization processes such as sputtering. The high degree of planarization facilitates the use of ultra-fine-line photolithographic methods. Other dielectric materials that are beginning to show promise include the following:

1. Fluorinated polyimides,[41] which have moisture absorption less than 0.5% (compared with standard polyimide in the 1–3% range).
2. Acetylene-terminated polyimides,[42] which show excellent planarization and can be formed in thicker layers in a single application.
3. Solventless epoxy resins (ultraviolet-curable cycloaliphatic epoxies), which show excellent planarization but have low thermal stability.[43]
4. An organic resin derived from benzocyclobutene, which offers a lower cure temperature than polyimide (i.e., 250°C compared with ≥350°C for polyimide), a lower dielectric constant ($\epsilon_r \approx 2.60$), and a compatibility with standard thin films[44] (see entry in Table 9). Benzocyclobutene is also available in a form that can be photoimaged.[45]

Using polyimide as an interlayer dielectric for multilevel circuits necessitates the fabrication of vias in the dielectric to connect different conductor layers. With photosensitive polyimide precursors, via holes can be patterned directly by applying the precursor, exposing the substrate to UV light, developing away the unexposed portion of the precursor film, and curing at high temperature. Fabricating via holes in traditional polyimide that cannot be photo-imaged involves wet chemical or dry etching techniques. Wet chemical etching is performed on either fully or partially cured polyimide using standard

photoresist processing, whereas dry etching is done on fully cured polyimide using either plasma etching, reactive ion etching, or reactive ion milling.

SUMMARY

The Laboratory has a strong program in the investigation of advanced materials and their application to electronic packaging structures, especially multichip modules.

Multichip modules are becoming the mainstay of modern high-performance packaging. Many complex multilayer structures, which contain a combination of several materials, are required to address the diverse application areas of today's electronic technology. High-performance materials and stringent process control are required to execute a viable multichip module technology successfully. Materials and structures that currently play a major role in multichip module technology are aluminum nitride and silicon for substrates, polyimide for dielectrics, copper metallization systems, bumped solder joints and TAB interconnects, and Parylene and urethane overcoats. These materials and structures, which have been appropriately modeled and analyzed by APL researchers to ensure optimum performance and reliability, are the basis of APL's advanced packaging technology today. In the future, the use of materials such as diamond may be extremely important in thermal management. Laser formed (laser reflow) or deposited interconnects may provide the ultimate flexibility while maintaining high density, electrical performance, and reliability.

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ACKNOWLEDGMENT: I would like to thank all my colleagues in the Microelectronics Group and the Materials Laboratory who contributed to the information in this article. A special thank you is given to S. Lynn Hoff and Heather L. Hall for word processing of the manuscript and to Murrie W. Burgan for her helpful suggestions.

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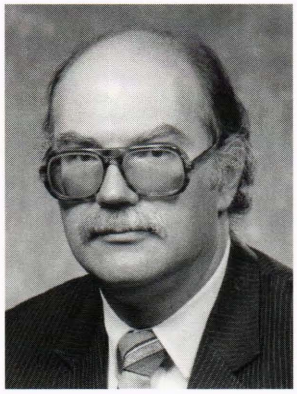

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