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MICROELECTRONICS AT APL: THE FIRST QUARTER CENTURY*

In the ongoing integrated electronics revolution, with millions of transistors now being placed on a single square centimeter of silicon, the need to harness these powerful chips and combine them with other devices to form workable electronic systems is paramount. APL's Microelectronics Group is providing many of the designs, assembly methods, testing tools, and services necessary to weld the new technology into electronic systems for space science, avionics, biomedicine, and ocean science.

INTRODUCTION

The Microelectronics Group was organized in 1960 to allow APL to participate actively in the rapidly advancing field of electronics miniaturization that was destined to play such an important role in the future of electronics. A report to the Director[1] recommended that APL establish a program in the field of microelectronics that should include

1. A microelectronics laboratory capable of fabricating functional circuit blocks and systems;
2. Research and development in materials, circuits, mechanical design, interconnections, and solid state applications;
3. System design involving the applications of microelectronics, considering such related areas as thermal problems, radiation damage, power supplies, and transducers;
4. Liaison and subcontracting.

Early tasks for the group included research on thin films and the fabrication and technology of electronic packaging and integrated circuits.[2] Later, as the capabilities of the group developed and the need to incorporate microelectronics into all electronic activities became paramount, efforts were focused on designing and producing circuits directly for a variety of APL programs. Initially, hybrid microcircuits were developed to satisfy the needs of growing and expanding space programs at APL. It was necessary to create high-density electronics to conserve precious payload volume and weight, as well as to provide reliable performance with minimum power consumption. Selective miniaturization was the goal of the group, with certain repeated circuit entities targeted for initial hybridization.

The first major circuit developed (1966) was the source-sink driver, which was designed to supply switching currents for the ferrite core memory of early Transit satellites. A schematic diagram and a photograph of this early hybrid circuit are shown in Fig. 1.

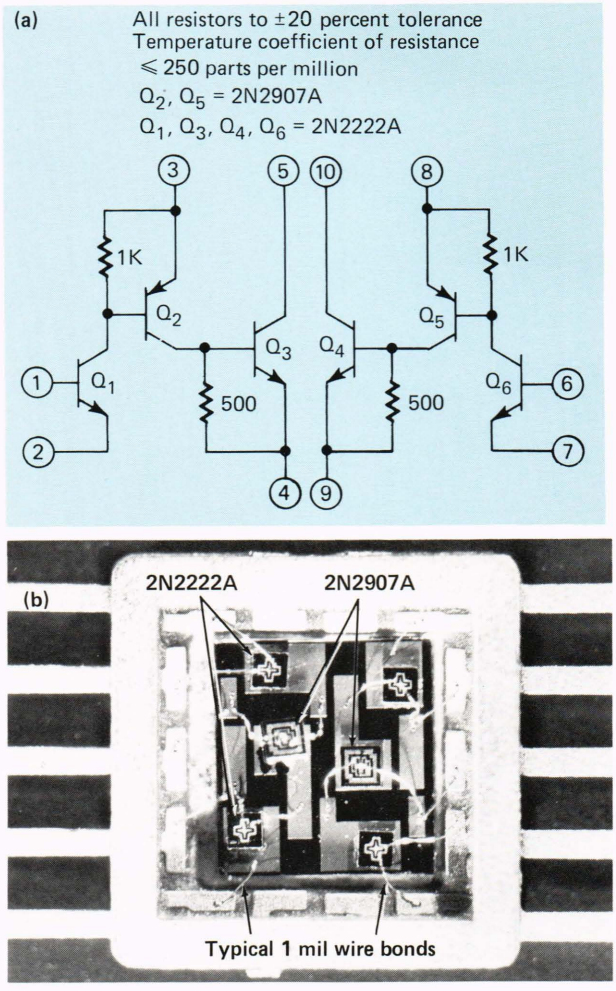


Figure 1—The source-sink driver hybrid was the first developed at APL for microcircuit space applications. Over 500 have been used on Transit satellites. (a) Circuit schematic; (b) photograph of an early hybrid prior to lid sealing.

The circuit consisted of thin-film chromium resistors on a glass substrate, with discrete bipolar transistor chips soldered to gold pads. Conductors on the substrate were photolithographically etched from a

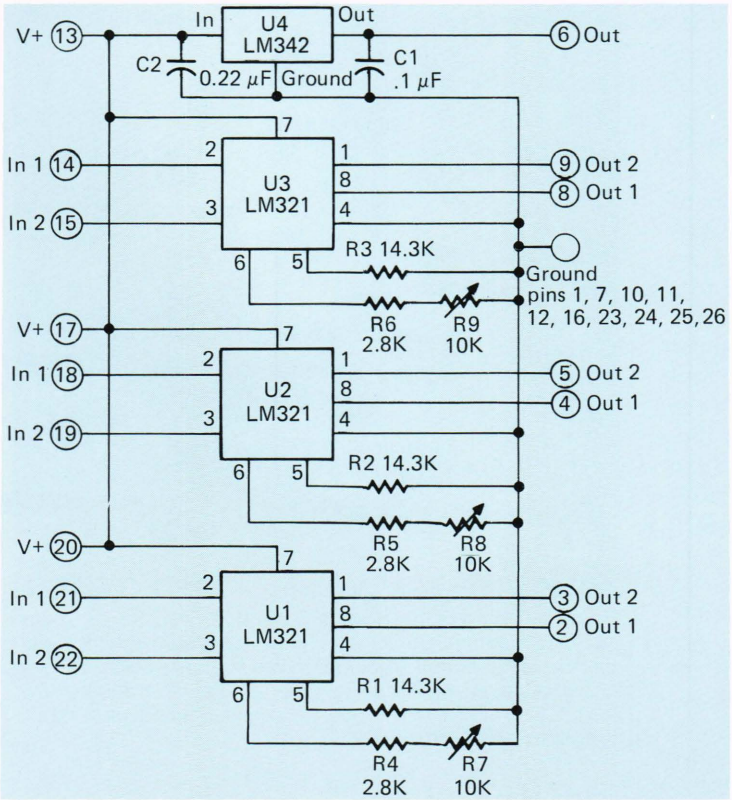
*The technical terms in this article are included in the Microelectronics Glossary that appears after the references.

deposited aluminum thin film. Interconnection wiring to both the transistors and substrate conductors was accomplished with thermocompression-bonded 25.4 micrometer (1-mil) diameter gold wire. The entire device was sealed with solder in a 10-lead 9.5 by 9.5 millimeter flat package in a nitrogen atmosphere. Fifty-two circuits were used on each Transit satellite; over 500 have now been launched into orbit with no known failures.

The simple building-block hybrid has continued to evolve over the years, finding its way into many nonspace applications such as avionics, biomedicine, and oceanography. Figure 2 shows a more recent hybrid circuit (1981). It was designed as a preamplifier to an accelerometer and was used in an underwater experiment. Here the package is much larger, 38.1 by 50.8 millimeters, and contains four analog integrated circuits (ICs), nine precision trimmable resistors, and two ceramic capacitors. While the resistors of the source-sink driver were built to ±20 percent tolerances and had temperature coefficients of resistance (TCRs) of ±250 parts per million per degree Celsius, the resistors in this modern circuit have tolerances of ±1 percent and a TCR of less than 25 parts per million per degree Celsius. To enable this unit to survive the undersea pressure environment, the accelerometer was hermetically sealed after being filled with a fluorocarbon liquid instead of the usual dry nitrogen gas. It can withstand pressures as great as 20 atmospheres.

As hybrid technology advanced, more complex circuit building blocks were designed with hybrid circuits; they were constructed with methods and components selected to withstand such harsh environmental factors as space radiation. Figure 3 shows a hybrid device, fabricated in 1980, that uses radiation-hardened, custom ICs, designed in cooperation with the Sandia National Laboratories. The four complex large-scale ICs are intraconnected on a ceramic substrate patterned with thin-film gold conductors. Prior to this hybrid design, the approximately 32 discrete ICs needed to perform the function occupied a 15.2 by 15.2 centimeter circuit board. The detailed schematic is quite complex: essentially the circuit serves as four 24-bit accumulators, multiplexed to an 8-bit, tri-state bus for transfer of 96 bits of experimental data to a microprocessor in twelve 8-bit bytes. Several of these devices were flown in the AMPTE program,[3] with dozens more scheduled to accompany the Galileo and Solar Polar missions.

As the packaging for space applications matured—with the need for high density, low power, and high reliability—it became evident that the same technologies could be used in the biomedical field for implantable electronic devices to stimulate, inhibit, and medicate the human body. The group has participated in the design, fabrication, assembly, and testing of several sophisticated biomedical systems, beginning in the 1974 era with the rechargeable pacemaker,[4] which



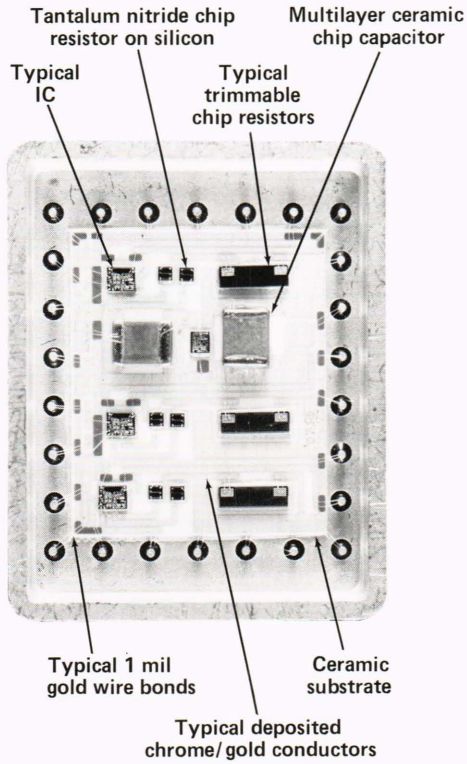


Figure 2—The accelerometer hybrid, recently developed for an APL underwater program, contains precision trimmable resistors and is packaged to withstand high pressures. The hybrid circuit measures one inch from top to bottom.

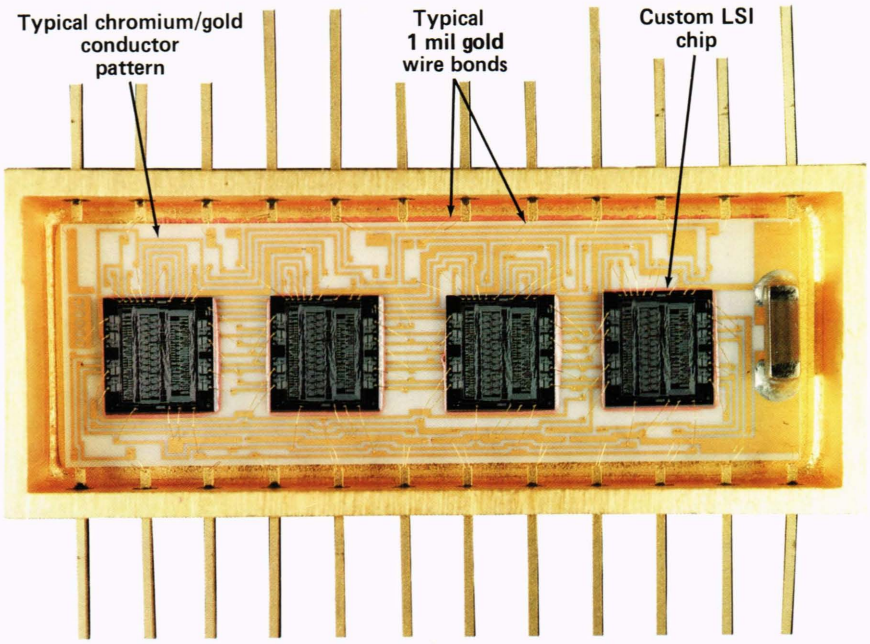


Figure 3—The accumulator hybrid, recently developed for APL space programs, contains four radiation-hardened large-scale integrated circuits and is used in the Galileo, Solar Polar, and AMPTE programs.

was designed to obviate the need for repeated pacer explants to replace batteries, and is continuing with such systems as the Programmable Implantable Medication System (PIMS)[5] and the Self Injurious Behavior Inhibiting System (SIBIS).[6] Figure 4 shows a highly complex hybrid developed in 1978 for an implantable neurological stimulator. The hybrid contains 34 medium-scale ICs (with approximately 50 logic gates each) plus one chip resistor. The electrical intraconnect is so complex that the substrate conductor pattern had to be implemented on seven separate conductor layers using a thick-film ink screening process. In addition, 640 individual wires were necessary to complete the connection process.

Figure 5 shows the controller board portion of PIMS. The board includes a complete microprocessor-based system implemented with large-scale ICs in ceramic chip carrier packages, which are soldered to a multilayer ceramic board containing three conductor levels. Also in the PIMS implant module is a miniature telemetry and command link for maintaining program control and monitoring the performance of the implanted system. The command and telemetry link is established by a hand-held unit that the patient can use for program modifications. However, major modifications are executed via the command link, which is controlled by a special personal computer system supervised by the physician. One of the two hybrids used in the PIMS command and telemetry link is shown in Fig. 6. The completed implantable system consumes only 20 microamperes from a 4-volt lithium battery and is expected to operate in vivo for more than seven years.

The evolution of medical hybrids and assemblies reflects the trends in all the miniaturized electronic systems developed at APL. In the last 10 years, chip and substrate densities have increased several orders of magnitude. An example of this change is shown in Table 1, which summarizes the important parameters for the major medical systems.

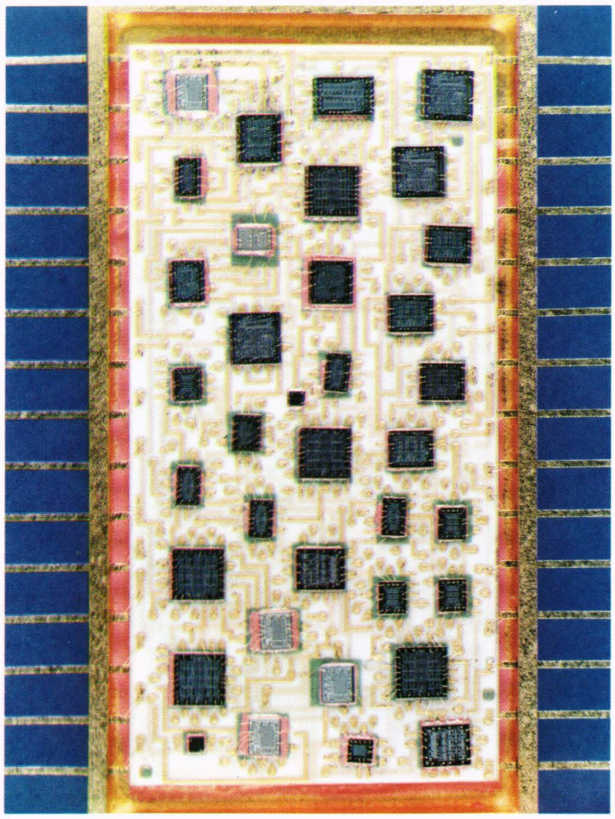


Figure 4—The Human Tissue Stimulator (HTS) hybrid was the first thick-film hybrid design developed at APL for the biomedical HTS implant. The unit shown is one of three designs in the HTS system. The pulse generator contains 32 medium-scale ICs, over 600 wire bonds, and was fabricated on a seven-conductor-level substrate.

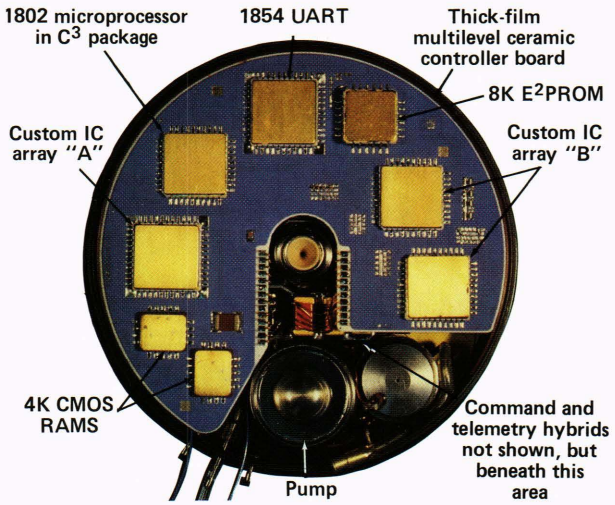


Figure 5—The Implantable Programmable Infusion Pump (IPIP) system. The central feature is the multilevel (three conductor layers) thick-film, surface-mount, controller-board assembly. The controller board contains a microprocessor, a universal asynchronous receiver/transmitter (UART), a random access memory (RAM), a read-only memory (ROM), and three custom-designed silicon gate arrays, mounted in solder-attached ceramic chip carriers.

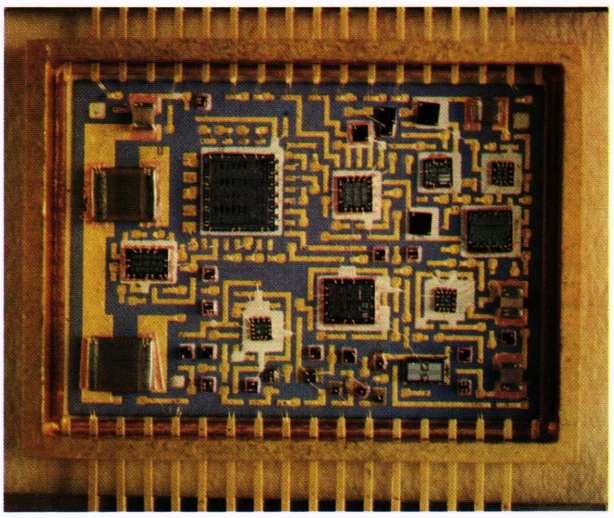


Figure 6—The heart of the IPIP command and receive communications link consists of two thick-film multilevel hybrids containing APL-developed gate arrays. The units are self-powered, deriving their operating energy from an external interrogation signal. The hybrid is shown above.

In response to these changing technologies and requirements, the Microelectronics Group has developed new technologies for the design, packaging, fabrication, and testing of microelectronic components, circuits, and systems. Recent efforts have led to greater use of thick-film multilayer substrates; ceramic chip carriers; nickel-chromium deposited resistors; the computer aided design (CAD) of hybrids; custom IC designs using gate array techniques, organic adhesives, and coatings; and improvements in reliability and quality assurance procedures. Table 2 summarizes generic group capabilities with important equipment and/or processing techniques.

It should be pointed out that the Microelectronics Group uses existing microcircuits, microchips, and standard technologies whenever possible. Frequently, however, an APL design or application calls for unique requirements such as small size, low power, extraordinary performance, special environmental requirements, or unique construction materials. While many commercial microelectronics organizations could satisfy these unique needs, they normally are unwilling to accept such a task because (a) the device is usually of high risk and frequently of low yield, (b) the production run (usually 1 to 20) is too low to warrant significant engineering costs, (c) extensive engineering is required and close cooperation between designers and system engineers is necessary, and (d) production processes are fixed and the relatively small production run does not warrant "tweaking" the process.

DESIGN

The Microelectronics Group has been actively engaged in the design and development of miniaturized devices, circuits, and subsystems for use in the varied and sometimes hostile environments encountered by APL instrumentation systems for space, underwater, and biomedical applications. Design capabilities range from simple analog and digital electronics to full microprocessor-based instrumentation and measurement systems containing several million bits of memory. The general emphasis in the design process is one of small size, low weight, low power, and complete systems testability. Consequently, many of the designs use complementary metal oxide semiconductor (CMOS) chips combined with standard hybrid and surface-mount layout and assembly methodologies. The integration of multiple chips and many circuit functions onto single pieces of silicon via gate array, standard cell, and full custom techniques is a driving focus of current and future design activity. These techniques have resulted in self-powered communication links and digital computer controllers that operate in the 10 to 100 microwatt range. Other circuitry has been developed to provide the optimum in low noise, fast response, and high data throughput.

The design process begins by consulting the program engineer to establish system requirements and by selecting an appropriate manufacturing technology (e.g., gate array, hybrid (thick or thin film), and multilayer circuit boards with ceramic chip carriers). Working from either a schematic diagram or a system specification, a design is generated (and breadboarded if necessary). Emphasis is placed on a design that uses computer-aided engineering (CAE) workstations such as the Mentor Graphics System (Fig. 7), which has recently been installed in the microelectronics design area and is linked, via an Apollo net, with other units in the Laboratory's CAD and drafting facility. Once checked, using both manual and machine simulation techniques, a layout for the miniaturized circuitry is

Table 1 — Evolution of microelectronic-based medical systems.

Design Description	*Hybrid Size (inches)*	*System Volume (in^3)*	*Substrate Process*	*Chip Carriers*	*No. Hybrid I/Os*	*No. Wire Bonds*	*Discrete Transistors*	*Total ICs*	*Universal Arrays*	*Logic Gates Total/No. per IC*
1974										
Two-speed fixed rate pacer										
Pacer hybrid[1]	0.75×0.75 ×0.15	0.084	Single-layer thin-film gold	—	12	49	4	—	—	—
1978										
Human tissue simulator										930/14
Command decoder hybrid[2]	0.84×1.65 ×0.14	0.205	Multilayer thick-film gold	—	30	557	14	21	—	
Pulse generator hybrid[2]	0.84×1.65 ×0.14	0.205	Multilayer thick-film gold	—	30	493	0	34	—	
Power output hybrid[2]	0.84×1.65 ×0.14	0.205	Multilayer thick-film gold	—	30	560	20	13	—	
1981										
Implantable infusion pump										15,000/500
Controller board	3.0 dia. ×0.15	1.059	Multilayer thick-film platinum/gold	8	23	275[5]	0	8	3	
Hybrid board assembly	2.0×2.0 ×0.15	0.600	PWB polyimide	1	30	—	0	1	0	
Hybrid 1[2]	1.0×0.75 ×0.15	0.113	Mutilayer thick-film gold	—	20	224	3	9	1	
Hybrid 2[2]	1.0×0.75 ×0.15	0.113	Multilayer thick-film gold	—	31	273	2	8	1	
1983										
Self-injurious behavior inhibiting systems										3700/900
Sensor hybrid[3]	1.27×0.77 ×0.16	0.156	Multilayer thick-film gold	—	24	185	0	2	1	
Stimulus hybrid[4]	1.27×0.77 ×0.16	0.156	Multilayer thick-film gold	—	24	202	0	2	1	
1984										
Implantable defibrillator										200,000/ 10,000
Hybrid 1	2.7×0.76 ×0.35	0.718	Cofired alumina with tungsten	4	30	95[5]	13	4	0	
Hybrid 2	1.25×2.7 ×0.30	1.215	Cofired alumina with tungsten	7	36	372[5]	0	7	3	
Hybrid 3	2.0×1.25 ×0.16	0.400	Cofired alumina with tungsten	5	15	96[5]	3	5	1	
Hybrid 4	1.25×2.0 ×0.30	0.750	Cofired alumina with tungsten	3	39	243[5]	8	3	2	

[1]Platform package
[2]Flatpack package
[3]Deep drawn package
[4]Unibody package
[5]Wire bonds are in surface-mounted ceramic chip carriers

generated using CAD drafting techniques. Two Computervision CAD terminals, located within the microelectronics facility, provide continual interactive layout support for all group design projects. Steps are being taken to improve the autoroute and autoplacement routines, originally designed for printed-circuit-board work, resident in the Computervision system. The ultimate goal is the automatic layout of hybrids and dense multilevel thick-film surface-mount assemblies. Mask-level, pattern-generation tapes for gate arrays and higher-level silicon integrated devices are generated using CAE methods for subsequent shipment to mask houses and semiconductor foundries.

The output of the CAD process consists of working schematics, parts lists, assembly drawings, and magnetic tape for use in the photoplotting and photoreduction operations. These outputs are reviewed with the program engineer to ensure product-requirement

Table 2—Microelectronic capabilities, equipment, and processes.

Function	*Description*
Electronic circuit and system design	Digital and analog—DC to 1 gigahertz Gate arrays and custom integrated circuits Limited antenna and microwave design capability
Microcircuit layout, fabrication, and testing	Thin-film hybrids—digital, analog, and power Thick-film hybrids—digital, analog, and power Surface-mount assemblies—ceramics (multilevel), stabilized organics, standard PCBs Specialized materials deposition—metals, dielectrics, polymers Limited semiconductor processing Coatings and adhesives—epoxies, polyimide, Parylene®, and Teflon® Micromachining, patterning to 1 micrometer Automatic electronic testing—programmable test system, circuits, probes, etc. Photo plotting and photoreduction Computer-aided engineering and drafting
Circuit qualification	Complete MIL-STD 883C qualification capability—thermal, mechanical, electrical
Circuit modeling	Thermomechanical and electrical modeling—finite element and difference techniques
Failure analysis and quality assurance	Electron microscope, energy-dispersive X rays, optical microscopes, profilometer, beta backscatter thickness measure, failure specialists, mechanical testers

compatibility. Following his approval and the receipt of required components, a prototype or engineering model is fabricated that provides proof of design and a check of form, fit, and function, and allows the generation of electronic and environmental qualification test plans. At this point, consultation with the program engineer is mandatory to assure product conformance and suitability to the initial requirements. Following that review (and assuming no design changes

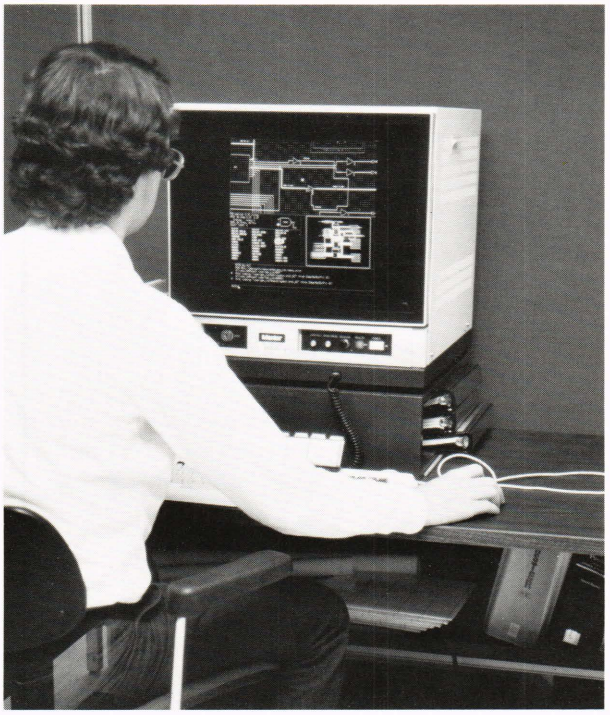


Figure 7—The Mentor DN660 Computer Aided Engineering Design/Graphics System.

are necessary), production of follow-on fully qualified units can begin. Figure 8 is a generalized flow chart for the design and development of a custom hybrid or surface-mount assembly. A similar flow sequence for the fabrication, testing, and quality assurance of the production models is presented below.

FABRICATION

The fabrication of hybrid and surface-mount assemblies is a highly complex science. It spans the full gamut from the precision manual handling of small components (items with dimensions as small as 200 to 350 micrometers are not uncommon) to the use of highly sophisticated automated assembly and analysis equipment (e.g., wire bonders, X rays, and scanning electron microscopes). The disciplines of electronics, mechanics, physics, chemistry, materials science, and metallurgy must be expertly interwoven to ensure the production of high-performance, highly reliable microcircuits. The anatomies of typical hybrid and surface-mount assemblies are shown in Figs. 9 and 10, respectively.

Materials

Appropriate materials and materials selection form the integral basis of any successful microcircuit application. Commonly used materials include alumina, glass, silicon, organic polymers, and metal clad structures for substrate materials; epoxies, solders, and polyimides for attaching chip and substrate; gold and aluminum wires and ribbons as well as solders and tape-mounted lead frames for chip-to-assembly inter-

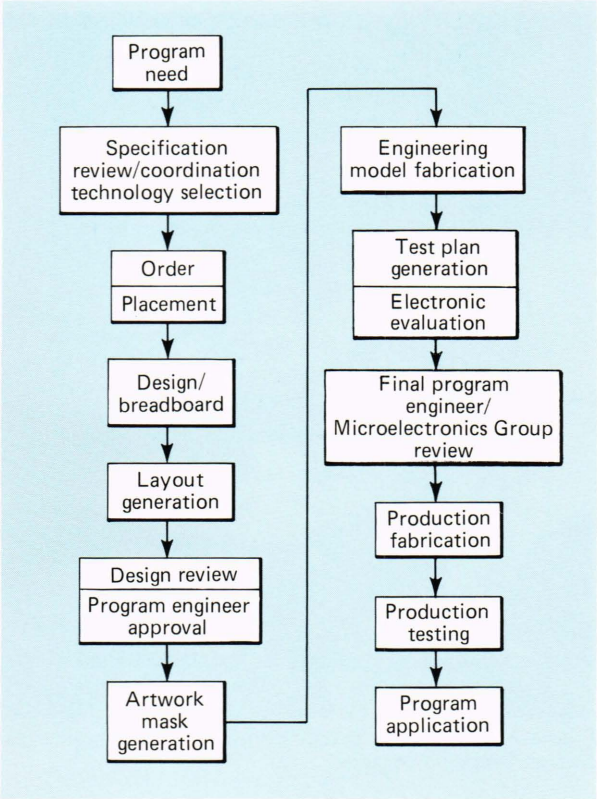


Figure 8—A typical custom hybrid/surface-mount assembly design and development flow sequence. The development of any custom miniaturized electronic assembly is a cooperative effort between the program user and the Microelectronics Group.

faces; and ceramic, Kovar®, nickel, glass, and stainless steel as packaging materials. Physical and chemical vapor deposition facilities are available for materials such as gold, aluminum, silver, nickel, chromium, nickel-chromium alloys, silicon monoxide, silicon dioxide, vanadium, tantalum, and titanium. Microplating, etching, and photolithography laboratories are maintained in addition to new experimental and production areas for the printing and firing of thick films. Materials used in these areas include gold, copper, and tin plating baths; acids, bases, and solvents; organic light-sensitive polymers; and conductive and nonconductive thick-film pastes of various metal/glass rheological combinations. Quality control of materials is a vital link in the success of any miniaturized electronic project; it is assured through extensive inspection, testing, and analysis. Techniques for analyzing and characterizing new materials involve the use of scanning electron microscopy, energy dispersive X rays, Auger spectroscopy, secondary ion mass spectrometry, atomic absorption, X-ray diffraction, etc.

Substrate Development

Two basic forms of substrate metallizations are used in hybrid and surface-mount assemblies: thin film and thick film. Thin-film substrates are produced by the vacuum deposition of thin metal or dielectric layers (e.g., 0.03 to 3 micrometers thick) over an entire substrate (ceramic, glass, silicon, etc.) and then photolithographically creating the desired design pattern by etching. Other variations of deposition through a mask and selective plating are also used to create thin-film

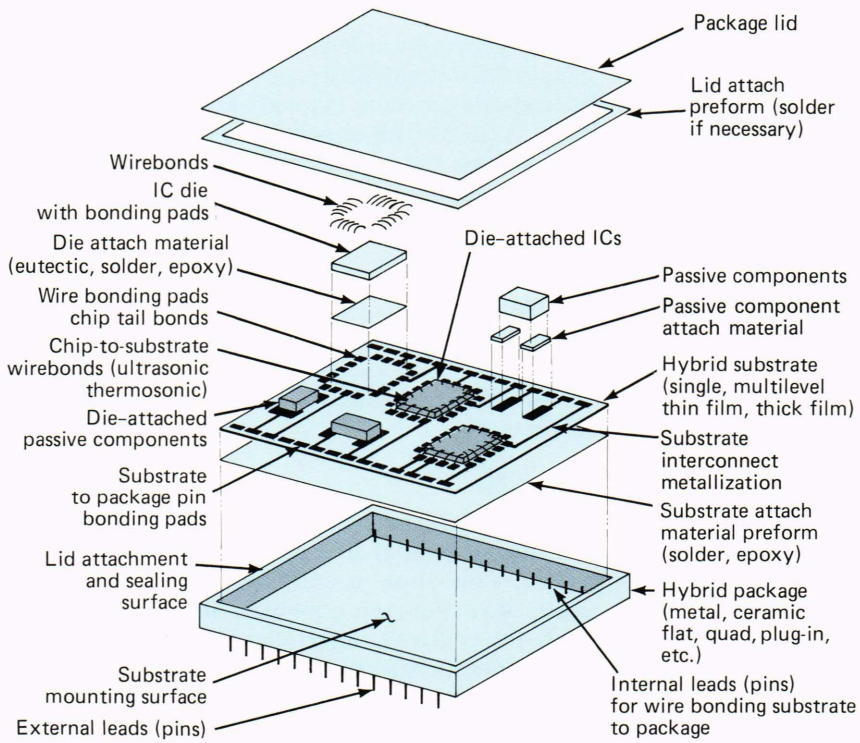


Figure 9—The anatomy of a chip-and-wire hermetic hybrid.

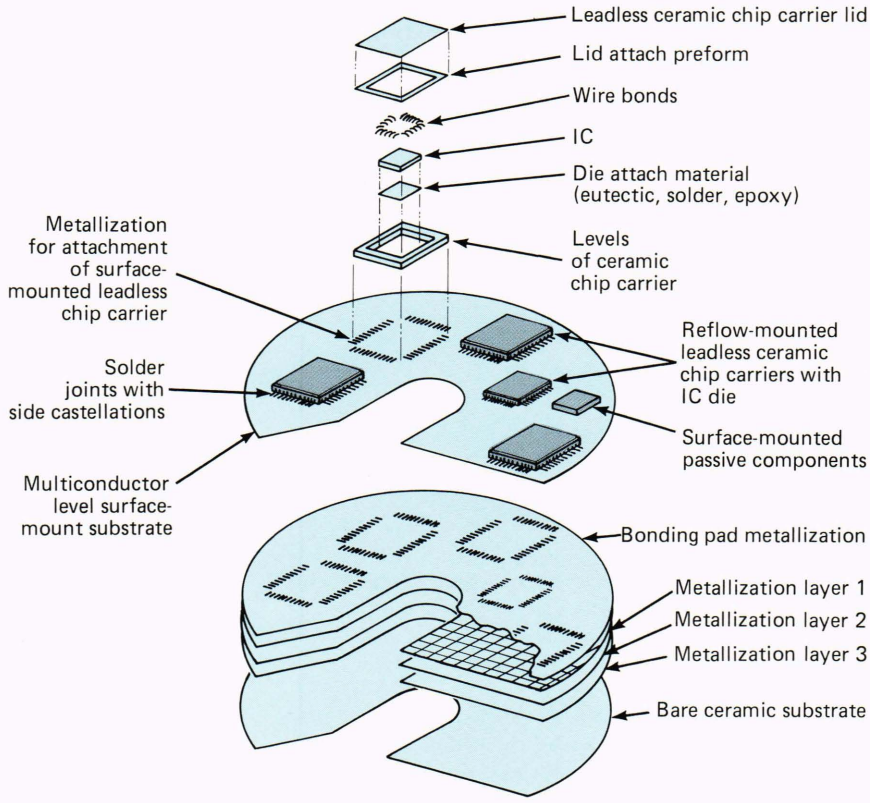


Figure 10—The anatomy of a surface-mount technology assembly.

substrates. Those substrates typically contain single-level metallization, although multilevel thin-film systems have been created using both glass and polyimide dielectric materials. Thin-film substrates can be seen in the hybrids shown in Figs. 1, 2, and 3.

Thick-film substrates are created by a screen printing process in which metal and/or dielectric ink is forced through a photolithographically patterned screen or stencil onto an underlying substrate (typically ceramic). The deposited ink pattern is dried and fired at temperatures between 600 and 1000°C to fuse the ink to the substrate. Multiple conductor levels can be made using intervening dielectric layers. Examples of thick-film substrates used in hybrids and surface-mount assemblies are shown in Figs. 4, 5, and 6.

In response to increasing demand, a new, modern facility has been created to fabricate thick-film hybrid and surface-mount assembly substrates. It is equipped with a modern screen printer and a thick-film firing furnace as shown in Figs. 11 and 12, respectively. After firing, the substrates will be tested completely for continuity/anticontinuity using a programmable flying test probe that is driven by direct input from the CAD system and will assure the high quality of APL's thick-film products.

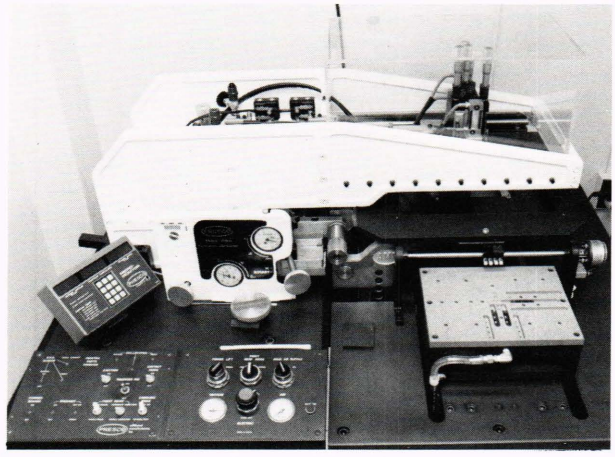


Figure 11—Semiautomatic screen printer for the deposition of thick-film conductor and dielectric links.

ASSEMBLY

Miniaturized electronic circuits are assembled using the chip-and-wire and the solder reflow techniques. Chip-and-wire assembly methods are best illustrated by the typical hybrid microcircuit anatomy shown in Fig. 9. A generic flow sequence for assembly, testing, and certifying a chip-and-wire hybrid assembly is shown in Fig. 13. Hybrid fabrication or assembly begins by bringing together pretested and qualified parts such as an integrated circuit die, passive components, a host package, and an interconnection substrate. The first operation involves the attachment of dies to the substrates and the incorporation of the substrates into the host package. There are several attachment methods, including eutectic die attach, solder reflow, and organic adhesives. These operations are scheduled so that the highest temperature processes are done first

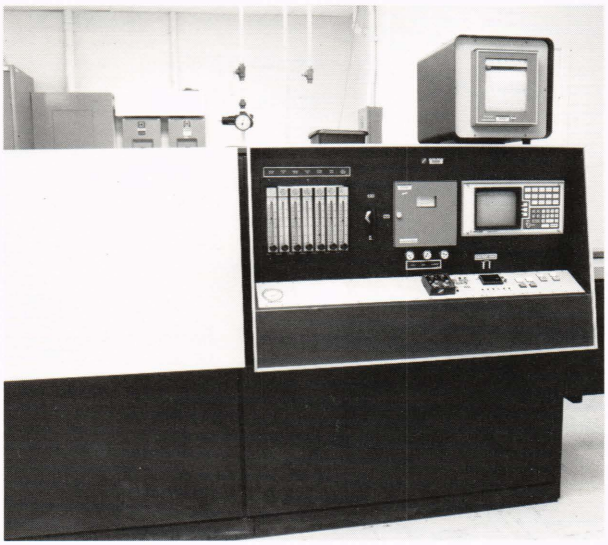


Figure 12—Microprocessor-controlled thick-film firing furnace. The unit is capable of temperatures above 1000°C with either an inert gas or an oxygen ambient.

and the lowest temperature process last. Following die and substrate attachment, wires are added using ultrasonic, thermosonic, and/or thermocompression wirebonding methods. After the wires are bonded, they are pulled nondestructively (to a preset limit) to ensure the success of the bonding operation. The nondestructive pull tests have done much to eliminate the occasional maverick bonds that appear in otherwise strong bond pull data. Representative bond pull strength distributions with and without prior nondestructive pull tests are shown in Fig. 14.

After wirebonding and electronic testing verification of the unlidded hybrid, the units are sealed under dry ambient conditions using either solder or seam welding; seam welding appears to be the best technique for the future. Figure 15 shows the Microelectronics Group seam welding system. The welding head is located inside an environmentally controlled enclosure, which maintains extremely low moisture conditions (less than 10 to 20 parts per million by volume). The unit is capable of handling round, square (rectangular), or other geometries simply by changing programming commands. It can handle package geometries up to 7.5 centimeters square with upgrades available for packages up to 15 centimeters square. Following the sealing operation, the hermeticity of the packages is checked using a helium sensitive mass spectrometer that can perform electronically tests for both fine and gross leaks. Electronic, thermal, and mechanical testing follows this operation. Figure 13 shows a typical test sequence.

Another major form of miniaturized assembly is solder reflow, which uses surface-mount technology. Typical surface-mount assembly methods are shown in Fig. 10; Fig. 5 shows an example of an APL surface-mount assembly. With this technique, solderable components such as passive devices, integrated circuits (packaged in leadless ceramic chip carriers), and hybrid packages are attached using hot-stage, furnace, or condensation soldering methods. Surface-mount assemblies offer ease of component replacement, testability, and medium-to-high density and lend themselves to automation. This method of assembly has already made significant contributions to many APL activities including the ultrastable 5 megahertz oscillator, the Dual Doppler Beacon, Virgo Program, PIMS, and

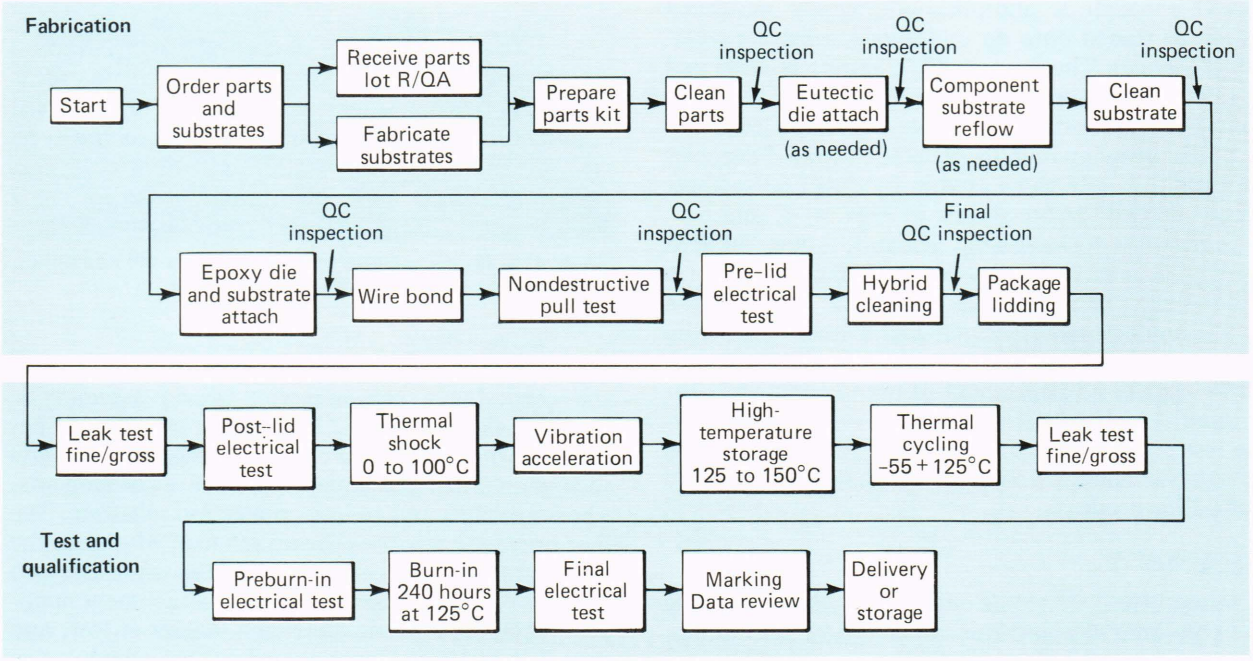


Figure 13—Typical custom hybrid fabrication, test, and qualification flow sequence.

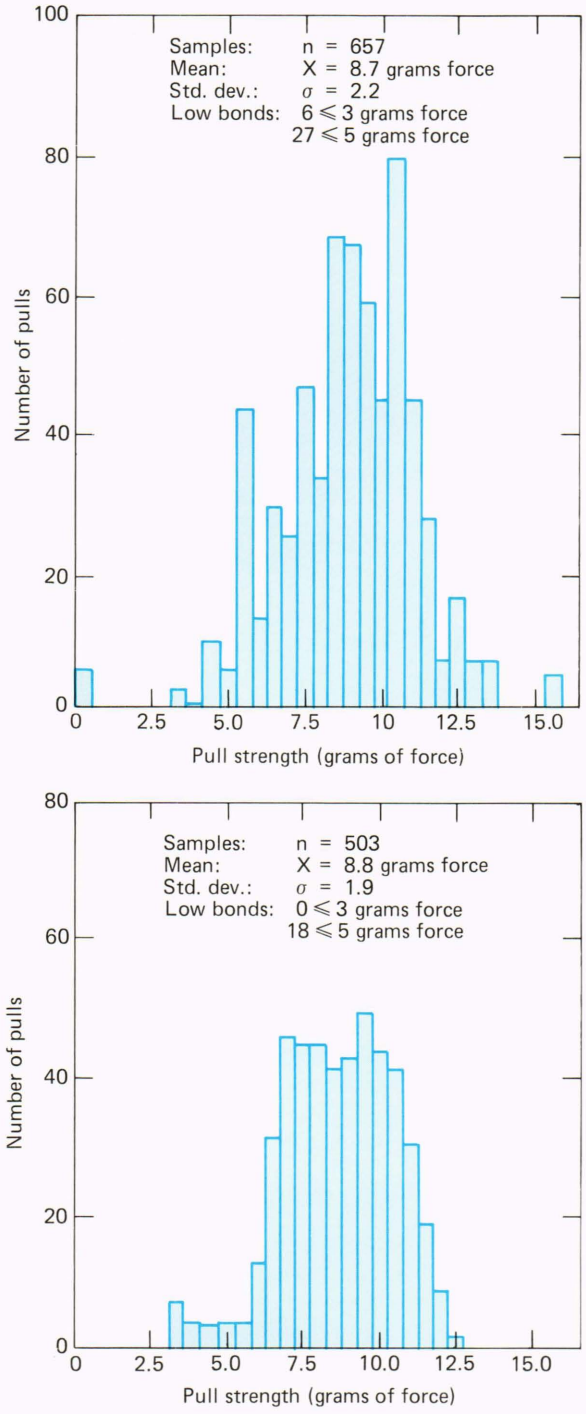


Figure 14—Wire-bond pull-test strength distributions. (a) Pull test conducted immediately after bonding; (b) pull test conducted after pretesting using nondestructive methods.

in the Ocean Data Acquisition Program. The technology will play an even more significant role in ongoing programs such as the Automatic Implantable Defibrillator and the TOPEX radar altimeter. In the surface-mount field, the leadless ceramic-chip carrier, multilevel thick-film substrate combination is particularly attractive because it provides not only ease of design, assembly, and test, but also extreme ruggedness and

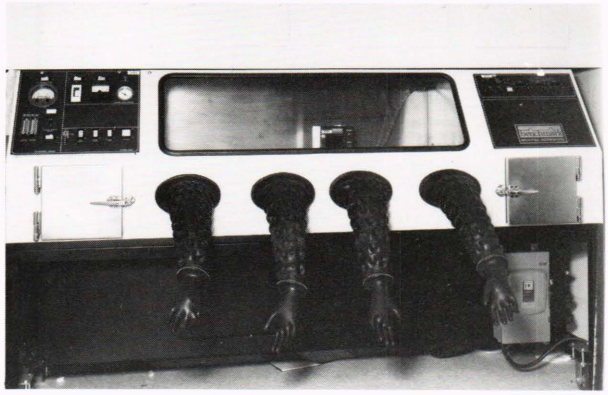


Figure 15—Package welding system. The benchmark seam sealing system is capable of welding or soldering hybrid packages in a dry inert gas environment.

reduced susceptibility to thermal and mechanical mismatch problems. Even greater thermal mismatches produced by high-rate power cycling can be overcome by the use of a proper board, assembly, and heat-sink design. The Microelectronics Group has investigated this field extensively over the last 5 years and has made several significant contributions to the field.[7-9]

The key to the success of any surface-mount project is the solder reflow operation. A vapor phase (condensation) soldering system has been installed recently that provides high-heat capacity, an extremely stable reflow temperature (determined by the boiling point of the FC-70 Fluorinert® liquid), and reduced solder surface oxidation (since all reflow takes place under an inert ambient atmosphere). The vapor-phase soldering equipment is shown in Fig. 16. After reflow, the surface mount assemblies are cleaned, inspected, and mounted on test fixtures for electrical testing.

PACKAGING/PROCESSING

Examples (hybrids and chip-carrier surface-mount assemblies) of standard miniaturized electronic packaging concepts developed and implemented have been described in previous sections. Because of the ever-increasing pressures of device integration, the packaging of individual devices and circuits is being replaced by the integrated miniaturized packaging of complete systems. Thus, package design, analysis, and fabrication capabilities have been expanded in several areas. Strong, rugged, and lightweight system enclosures can be fabricated routinely using chemical milling techniques. Figure 17 shows an example of a chemical milled package structure. Large-area multilevel board structures up to 230 centimeters square can be easily designed, modeled (mechanically and electrically), fabricated (either through subcontract or internally), assembled, and tested.

The prototype of the design for the TOPEX radar altimeter is shown in Fig. 18. The design of the thermal heat sink resulted from an extensive thermal analysis of the board. Various board materials and electronic components were combined into meaningful hybrid assemblies such as those being produced for the

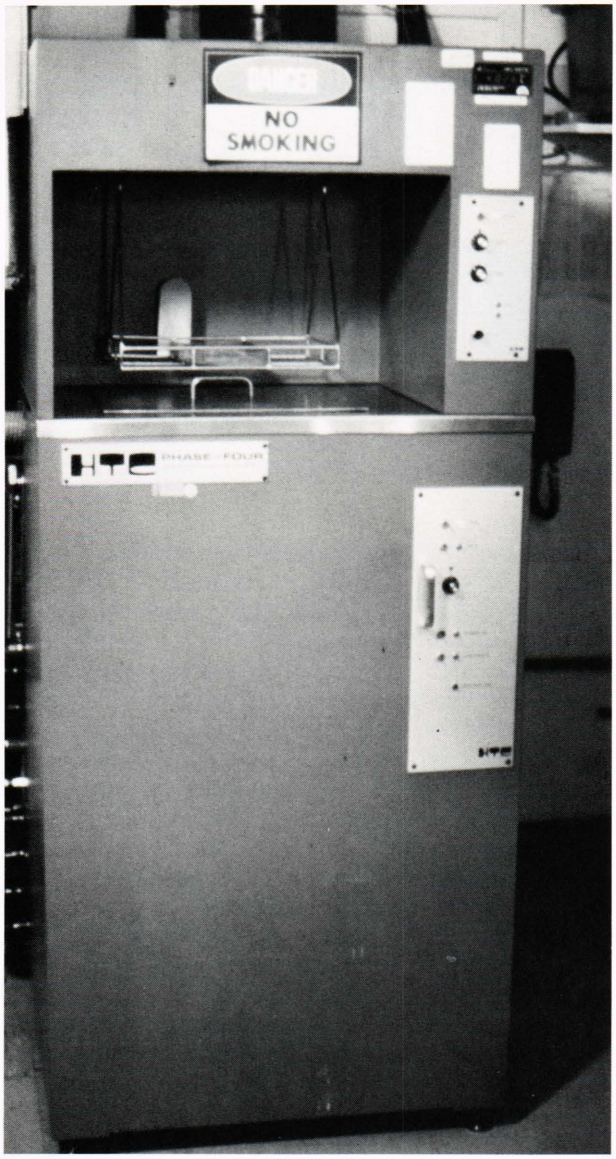


Figure 16—Vertical vapor phase soldering system. The HTC phase four system is capable of soldering boards up to 12 by 14 inches.

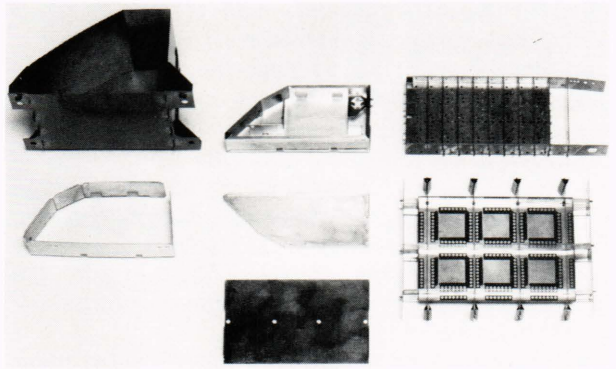


Figure 17—Chemical milled subsystem and system packages that were photolithographically patterned and chemically etched from thin brass and beryllium copper sheets. They are folded and held in place with tabs and/or solder. Packages produced in this manner are strong, lightweight, and, depending on design, hermetic.

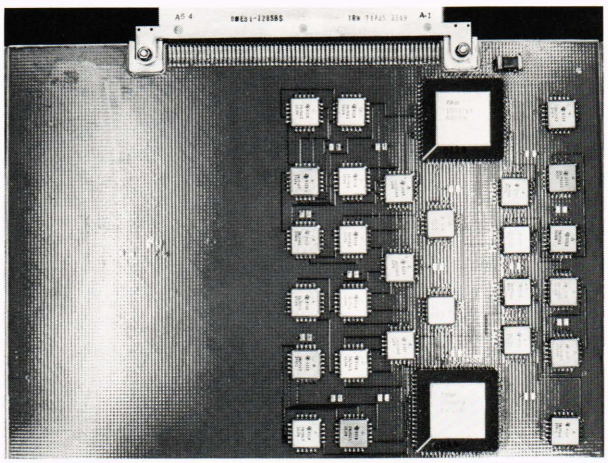


Figure 18—Integral heat sink chip carrier layout on the TOPEX radar altimeter. The TOPEX digital signal processing system will use hundreds of ceramic chip carriers mounted on large ceramic multilevel boards.

Virgo Program.[10] In that application, leaded commercial integrated circuits were combined with precision solderable thin-film chip components to form ultralow noise sensor amplifiers (Fig. 19).

Other program requirements not only involve miniaturized packaging but also require the development of unique processes, materials handling capabilities, and/or one-of-a-kind assembly procedures. For example, to this end we have developed a high-temperature brazing and Teflon® coating capability in support of the hydrogen maser program, electroless nickel plating of Fiberglas® for the Dual Doppler Beacon Program, polyimide dielectric layers for an NIH-sponsored multisensor site, neural implant device, tantalum and titanium anodization methods for undersea thermistor mounting and medical system sealing, and platinization to increase the effective conductor surface area for undersea electrodes.

RELIABILITY AND QUALITY ASSURANCE

The group's equipment and staff are constantly being upgraded to provide increased capabilities and improvements in the areas of reliability and quality. Activities in the area of reliability engineering include design review and reliability input to all specifications and proposals, personnel training, materials certification and vendor auditing, reliability prediction, failure data collection, analysis and reporting, and reliability research and development. Significant analysis and characterization capabilities have been established in support of its operation. New analytical equipment includes a scanning electron microscope (SEM) equipped with the latest full quantitative energy dispersive X-ray system (for materials identification). Figure 20 shows a SEM photomicrograph of an integrated circuit in a ceramic chip carrier. The essentially unlimited depth of field of the SEM is clearly illustrated as one traces the 25.4-micrometer-diameter gold interconnect wires from their origin at the bond-

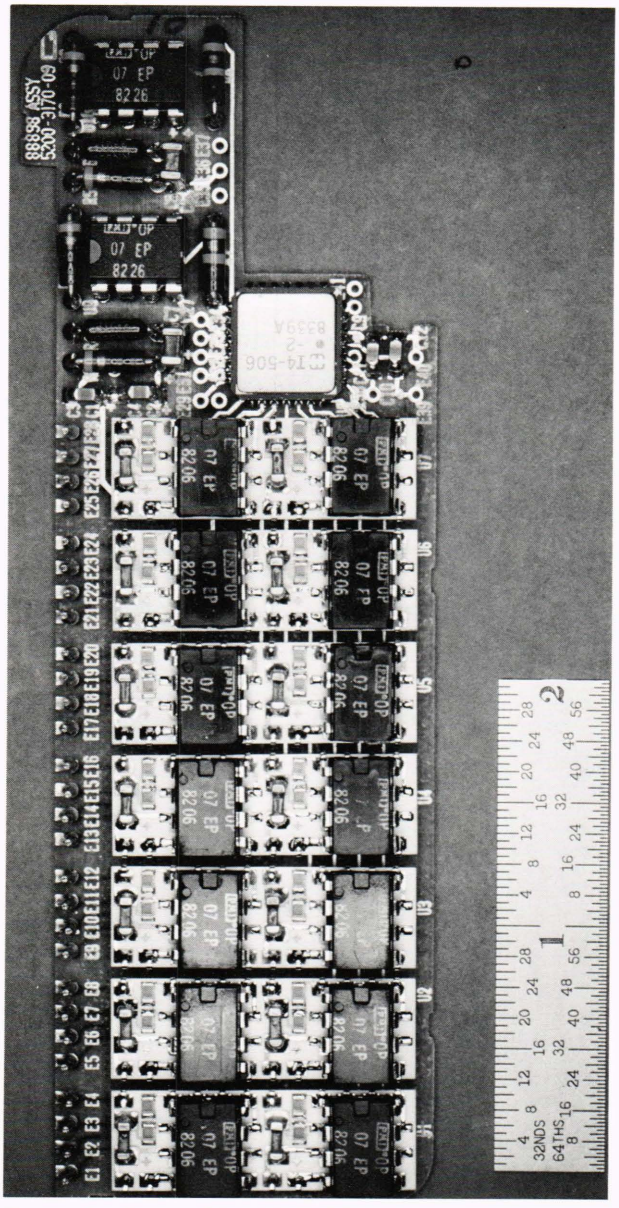


Figure 19—Preamplifier assemblies used in the Virgo Program. The preamplifier boards combine leaded and leadless components in a compact prototype assembly. The meaningful mixing of miniaturized electronic technologies has allowed creation of a high-performance unit that can be easily assembled.

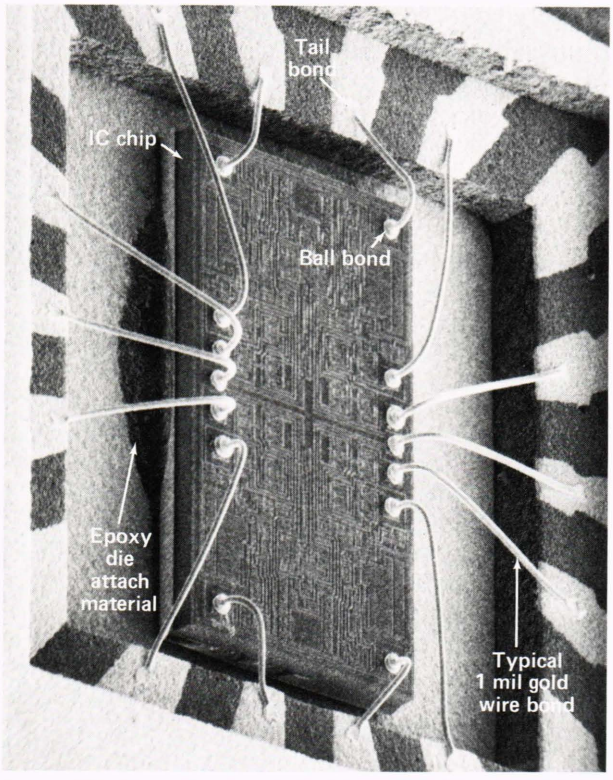


Figure 20—Scanning electron photomicrograph of an integrated circuit die in a ceramic chip carrier.

ing pads on the integrated circuit to their terminals on the chip carrier "lead" frame.

Other quality assurance and analysis capabilities include optical microscopy; mechanical, electrical, and chemical test methods; and the ability to qualify miniaturized electronic assemblies to military standards of reliability (MIL-STD-883C) through the application of a controlled battery of mechanical, electrical, and thermal stressing methods. A typical high-reliability qualification sequence is included in the flow chart in Fig. 13.

Reliability and quality assurance activities make full use of Auger electron spectroscopy, secondary ion mass spectrometry, residual gas analysis, and atomic absorption techniques in the conduct of failure analysis and materials certification studies. Close cooperation and collaboration have been maintained in APL's Research Center where the advanced materials analysis tools reside. Because precision component procurement and acceptance testing prior to assembly are important parts of the success of any miniaturized electronics program, group personnel work closely with vendors, the APL Space Reliability Group, and outside professional experts to develop effective procurement quality assurance testing methods. Such cooperation was evident in a recent capacitor end cap problem where joint testing and analysis procedures were developed[11] to assure component viability.

FUTURE MICROELECTRONICS AT APL

In the future, it is anticipated that microelectronics activities at APL will continue to provide a wide variety of unique and exciting developments. A 5-year modernization plan[12] has been developed for enhancement of all of the facility capabilities previously described. With the tools and processes to be acquired or developed in the next five years, APL's microelectronic technology should be well prepared to meet the challenges of the 1990s.

A major focus of the plan includes a thrust into VLSI/VHSIC technology, including development of CAD/CAE tools for the rapid design and analysis of custom circuits at the Laboratory in cooperation with the Laboratory's Computer Aided Design Group. A

facility for gate array processing, where only top-level intraconnect metal must be etched, will be developed in-house for low-cost, quick-turnaround needs. Costs of less than $5000 per design and turnaround times of less than 2 to 4 weeks are anticipated for arrays initially of 1000 to 2000 gates. The technique is expected to be extended to arrays of 20,000 gates per chip using the CMOS technology and can be applied possibly to 5000 gates per chip on gallium arsenide arrays where high-speed performance and radiation hardening are required.

Other custom designs using a standard cell or full custom design approach will be developed using extensions of some of the CAD/CAE tools acquired from the University of California at Berkeley and the University of Washington. The design tools are currently being used in the APL Space Department[13] and the Technical Services Department. Processing of these custom designs will be accomplished at selected "silicon foundries" as required.

A second major thrust of the plan is to extend hybrid-circuit technology to meet the challenges of the 1990s. In this area, we will be introducing newer and denser substrate technologies in order to handle the higher number of inputs/outputs and interconnections. Potential candidates for these needs are multilevel cofired ceramics, multilevel thick films, multilevel polymers, multilevel thin films, or embedded wire techniques. On a selected basis, processes will be improved and automation will be introduced. Generally, automation will be applied to achieve better process controls, higher densities, and results and quality not possible with manual systems.

As the dimensions of electronic devices continue to shrink, increased emphasis on materials, quality, process control, and cleanliness will become paramount. Consequently, major efforts will be devoted to improving clean areas as well as to many aspects of reliability and quality control. In support of some of these needs, a new building, planned for 1988, will include modern cleanroom facilities and special laboratories for microelectronic activities. Many of the newer and modern tools of reliability and quality assurance will be introduced and applied to the APL microelectronic efforts.

In summary, microelectronics is still one of the most rapidly growing technologies. The end of the rapid expansion of microelectronic capabilities and the development of microelectronic applications are not in sight.

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Mr. Wagner is a Senior Member of the IEEE, a member of the Components, Hybrids, and Manufacturing Technology Subgroup, and a member of the International Society for Hybrid Microelectronics. When not working in professional activities related to VLSI hybrid microelectronics with his home computer, he enjoys sailboat cruising or racing and ice boating on Chesapeake Bay.

A MICROELECTRONICS GLOSSARY

– A –

Alumina — Aluminum oxide (Al_2O_3); a high-quality ceramic compound used as a base material for most thick-film substrates and frequently as a thin-film substrate material.

– B –

Ball bond — The initial bond made in thermocompression or thermosonic gold wire bonding. So named because the starting end of the wire is flame- or arc-cut prior to bonding, producing a ball-shaped end. Also referred to as a "nail head" bond.

Beam lead — A chip or die with electrical contacts in the form of flat leads extending beyond the body of the device. The beams are an integral part of the basic device metallization.

Bipolar device — A device whose operation depends on the transport of holes and electrons. It is usually made of layers of silicon with differing electrical characteristics such as a bipolar junction.

Bumped chip — A chip that has on its termination pads a "bump" of solder or other bonding material that is used to bond the chip to external contacts. This allows for simultaneous bonding of all leads at once rather than one at a time as in wire bonding.

– C –

Ceramic chip carrier — A modern package system for semiconductor dice or hybrids possessing external solderable terminals usually on four sides for direct surface mounting on boards. The chip carrier has distinct performance and density advantages over conventional dual in-line packages.

Cermet — An acronym for material used in making thin-film resistive components; derived from the words CERamic and METal.

Chip — The shaped and processed semiconductor die mounted on a substrate to form a transistor or other semiconductor device.

Chip and wire — Hybrid construction using multiple semiconductor dice interconnected to the substrate or package by means of wire bonds.

Complementary transistors — Two transistors of opposite conductivity (pnp and npn). Also applied to N-MOS and P-MOS transistors.

Conductor — A substance, body, or other medium that is suitable to carry an electrical current.

Crossover — A point where one conductive path crosses another; the two paths are insulated from one another by an intermediate dielectric layer.

– D –

Die (dice) — So named because the circuits are batch-fabricated by diffusion processes on a silicon wafer. The wafer is then "diced" or cut into individual components. Also called a "chip." Examples: transistors, diodes, ICs, resistors, capacitors, etc.

Die bonding — Process in which chips are attached to a substrate. In the attachment of a die to a gold base, the process creates a gold/silicon eutectic bond between the die and base. Other forms of die bonding include epoxies and solders.

Dielectric — Material such as mica, paper, or plastic film that has poor electrical conductivity and serves as an insulator. In many microcircuits, the dielectric is glass.

Diode — A device containing an anode and a cathode. Current flows in only one direction and is inhibited in the other direction.

Discrete — A separate and recognizable component, such as a resistor or capacitor. Alternatively, a semiconductor containing only one active device, such as a transistor.

Doping — The addition of impurities to a semiconductor to achieve a desired characteristic. Common doping agents for silicon include aluminum, antimony, arsenic, boron, gallium, indium, and phosphorus.

Dual in-line package (DIP) — The most common type of IC package with two parallel rows of leads that facilitate through-hole insertion in PC boards.

– E –

Electron-beam lithography — Lithography in which the energy-sensitive film or resist is placed in the vacuum chamber of a scanning beam electron system and exposed by the electron beam under digital computer control. After exposure, the film undergoes conventional development and other production processes.

– F –

Field effect transistor (FET) — A transistor in which the resistance of the current path from the source to drain electrodes is modulated by applying a transverse electric field to the gate electrode between the source and drain. The electric field varies the thickness of depletion layers under the gates, thereby reducing the conductance.

Flat pack — An IC package that has leads extending from the package

in the same plane as the package, so that leads may be spot welded or soldered to terminals on a substrate or a printed circuit board.

Flip chip (bumped chip) — A semiconductor die having terminations all on one surface in the form of solder pads or bump contacts. After the surface of the chip has been passivated, it is flipped for attachment to the matching substrate.

Frit (glass) — Finely ground glass. A primary component of many thick-film pastes used to provide adherence to the substrate for powdered metals and metal oxides.

– G –

Gate array — A fully diffused and metallized semiconductor wafer containing a matrix of identical primary cells arranged in columns with routing channels between them. Semicustom circuit design is accomplished by defining the etching pattern (the interconnection pattern) for the metallization layer.

– H –

Hermetic seal — Permanently sealed by fusion, soldering, welding, or other means to prevent the transmission of moisture, air, or gas.

Hybrid microcircuit — Microcircuit in which thin-film, thick-film, or diffusion techniques are combined with separately attached semiconductor or passive chips to form the circuit function.

– I –

Insulator — A nonconducting material used for supporting or separating conductors to prevent undesired current flow to other objects. (See dielectric.)

Integrated circuit (IC) — An interconnected array of active and passive elements within a single semiconductor substrate that can perform at least one electronic circuit function.

– J –

Junction — The boundary between a p region and an n region in a semiconductor. Junctions permit current to flow in one direction much more easily than in the other. They provide the basis for diode and transistor effects in semiconductors.

– L –

Large scale integration (LSI) — ICs that generally contain 300 to 3000 gates on a single chip. This typically translates to about 10,000 devices on a single chip.

Leadless inverted device (LID) — A method of mounting a semiconductor die in a miniature ceramic holder for subsequent mounting in a hybrid circuit.

Leakage current — The undesirable flow of current through or over the surface of an insulating material or insulator.

Linear circuit — A network in which the parameters of resistance, inductance, and capacitance are constant with respect to current or voltage, and in which the voltage or current of sources is independent of or directly proportional to the outputs.

– M –

Mask — A thin patterned sheet that shields selected portions of a base during film deposition. Also used to shield photosensitive material during photo processing.

Medium scale integration (MSI) — Integrated circuits that have about 30 to 300 logic gates on a single chip. This usually relates to approximately 1000 devices on a single chip.

Metal oxide semiconductor (MOS) —Structure in which the insulating layer is an oxide of the substrate material. For a silicon substrate the insulator is silicon dioxide.

Monolithic device — A device whose circuitry is completely contained on a single die or chip, e.g., an IC.

MOSFET — Metal oxide semiconductor field-effect transistor (FET). A family of devices using field-effect transistors; current flow is through a channel of n- or p-type semiconductor material, controlled by the electric field under a gate. MOSFETs are unipolar devices characterized by extremely high input resistance.

– N –

N-channel — A conduction channel formed by electrons in a semiconductor, as in an n-type field-effect transistor (NMOS FET).

npn transistor — A bipolar junction transistor having a p-type base between an n-type emitter and an n-type collector. The emitter should be negative with respect to the base, and the collector should be positive with respect to the base.

n-type electron semiconductor — An extrinsic semiconductor in which the conduction density exceeds the hole density.

– O –

Ohms per square — See Sheet resistivity.

Operational amplifier (OP AMP) — A general-purpose IC used as a basic building block for implementation of linear circuit functions.

Overglaze — Coating layer of printed and fired glass; may be a solder barrier, a protective coating for resistors, or an insulator to prevent possible short circuits, as in the case of a wire bond crossing over a printed conductor.

– P –

Passivation — Growth of an oxide layer on the surface of a semiconductor to provide electrical stability by isolating the transistor surface from electrical and chemical conditions in the environment.

Paste (ink) — For thick film, a composition of micrometer-size polycrystalline solids suspended in a thixotropic vehicle. The solids are chosen for their electrical characteristics, i.e., metals for conductors, metals and oxides for resistors, and glasses for glazes and dielectrics.

Photoresist — Light-sensitive material deposited as a uniform film on a wafer or substrate. Exposure of specific patterns is performed through masking operations.

P-channel — A conduction channel formed by holes in a p-type semiconductor, as in a p-type field-effect transistor (PMOS FET).

p-n junction — A region of transition between p- and n-type semicon-

ducting regions in a semiconductor device.

pnp transistor — A bipolar junction-type transistor having an n-type base between a p-type emitter and a p-type collector.

p-type semiconductor — An extrinsic semiconductor in which the hole density exceeds the conduction electron density.

Purple plague — A brittle gold aluminum intermetallic compound ($AuAl_2$), purple in color, occurring at the bonding point of gold connecting wire and aluminum contacts. One of the five aluminum/gold intermetallic compounds associated with the bonding process.

– R –

Random access memory (RAM) — A data storage device having the property that the time required to access a randomly selected datum does not depend on the time of the last access or the location of the most recently accessed datum.

Read only memory (ROM) — A device for storing data in permanent, or nonerasable form. Usually a static electronic or magnetic device allowing extremely rapid access to data.

Resist — Material such as ink, paint, or metallic plating used to protect the desired portions of the printed conductive pattern from the action of the etchant, solder, or plating.

Rubylith — A laminate consisting of a thin red film with a heavier clear backing. Used to produce master artwork for thick-film patterns by scribing and peeling away portions of the red layer.

– S –

Screen printing — The basic thick-film deposition process in which the paste is squeezed through a fine mesh stencil screen to produce a prescribed pattern on a substrate.

Semiconductor — A material whose conductive ability lies between that of a conductor and an insulator. The most common types are silicon and germanium.

Sheet resistivity — The resistance of a unit area of printed and fired thick film or deposited thin-film material. Expressed in ohms per square per unit of film thickness.

Sintering — The process of bonding metal or other powders by cold-pressing into the desired shape, then heating to form a strong cohesive body.

Small scale integration (SSI) — ICs containing fewer than 30 logic gates on a single chip. This typically translates to less than 100 devices on a single chip.

Sputtering — Dislocation of surface atoms of a material bombarded by high-energy atomic particles.

Substrates — The physical material on which a microcircuit is fabricated. Used primarily for mechanical support and insulating purposes. However, semiconductor and ferrite substrates may also provide useful electrical functions. For thick films, the substrate is usually high-purity alumina.

Surface acoustic wave (SAW) — An acoustic or vibrational propagating wave localized to the surface of an oriented crystal. The propagation velocity of this wave is typically five orders of magnitude below that of an electromagnetic wave in free space. Can be used to form miniature delay lines or filters.

– T –

Thermocompression bonding — The joining of two materials by the combined effects of heat and pressure. In making this bond, the first termination is a ball bond while subsequent terminations of the same wire are stitch bonds.

Thick film — The deposition of resistor, dielectric, or conductor pastes on a substrate by screen printing, then firing at elevated temperature to drive off the binder and sinter the solids. Typically the thickness of a single layer is 10 to 75 micrometers though it may be greater.

Thick-film circuit — A microcircuit in which passive components of a ceramic/metal composition are formed on a ceramic substrate by successive screen printing and firing. Discrete active elements are attached separately.

Thin film — A film deposited on a glass, ceramic, or semiconductor substrate to form conductors, insulators, capacitors, resistors, or other circuit components. Thin films typically range in thickness from 0.1 to 3 micrometers.

Thin-film circuit — A circuit in which the passive components and conductors are produced as films on a substrate by evaporation or sputtering. Active components may be similarly produced or mounted separately.

Thixotropic — A property of a paste or liquid that describes its ability to flow more readily when agitated or sheared. Thixotropy of a paste is a necessary condition for screenability in thick-film operations.

Transistor — An active component of an electronic circuit consisting of a small block of semiconducting material to which at least three electrical contacts are made, usually two closely spaced rectifying contacts and one ohmic contact. It may be used as an amplifier, detector, or switch.

Trimming — The process of cutting away a portion of a thick-film or thin-film resistor in order to increase its value. Resistors can often be trimmed to within ± 0.1 percent of the desired value. Cutting is performed with an air abrasive tool or a laser beam. The width of the cut is called the kerf.

– U –

Ultrasonic bonding — A joining technique for wire and lead attachment that employs pressure plus an ultrasonically induced scrubbing action to form a molecular bond.

– V –

Very-large-scale integration (VLSI) — ICs that contain 3000 or more logic gates on a single chip. This generally results in more than 100,000 devices on a single chip.

Via — A conductive path typically made through a hole or opening in a dielectric layer used to connect conductor patterns on at least two levels of a multilevel board structure.

– W –

Wafer — A thin slice of silicon containing as many as 1000 semiconductor dice. These are separated by either scribing and breaking the wafer or by diamond sawing.

Wafer probing — An electrical test of devices on the wafer, using tiny probes to make contact with the metallized pads on the die.