

This paper discusses fundamentals of varactor multipliers, with the analysis primarily concerned with the case of a charge-controlled multiplier using an abrupt junction diode. The use of idler circuits to obtain high-order multipliers and various circuit configurations is examined. Several multiplier circuits used by the author are treated from the designer's point of view, and a practical satellite application is considered in some detail.

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The need for small, lightweight, reliable R-F power sources in communications systems has led to many advances in the field of solid-state devices. In recent years, advances in varactor diode technology have made solid-state UHF and microwave generators practical for such systems. Modern varactors can achieve high conversion efficiency and large power-handling capability. Single varactor circuits with power outputs of several watts in the low-gigacycle region are becoming commonplace. At the current rate of improvement in varactor technology many dramatic advances can be expected in the near future.

The Varactor Diode

The varactor is a p - n junction diode, with a reverse voltage applied, used as a capacitor. The diode depletion region expands with increasing back-bias voltage, and this causes a voltage variable capacitance effect. In the voltage region between forward conduction and reverse breakdown the capacitance voltage relationship can be expressed as

$$C = K(\phi - V)^\alpha, \quad (1)$$

where C is capacitance, ϕ is the contact potential, V is the applied voltage, and K is a constant of appropriate dimensions (farads per volt to the α). For applied voltages in the range near forward conduction, this expression is incorrect; however, for voltages of several volts in the back direction it is quite accurate. The exponent α ranges roughly from $-1/5$ to $-1/2$, depending on the impurity profile. In addition to the nonlinear capacity effect, the bulk and contact resistance of the semiconductor material lead to an additional resistance component. Since this resistance effect leads to loss in harmonic generators, it is desirable to hold it to a minimum. On the other hand, the power-handling capability of a varactor is proportional to

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the square of the breakdown voltage, as will be shown later. High breakdown voltage can be achieved with a low-impurity concentration. This leads to high resistivity, however; therefore, the semiconductor manufacturer will usually need to compromise between high power-handling capability and high efficiency. The simple equivalent circuit used to represent the varactor is shown in Fig. 1. The series resistance R_s is considered as constant. Although this is not strictly true, effects owing to its variation with voltage do not appear to contribute significantly to multiplier performance.



Fig. 1—Varactor equivalent circuit.

In addition to the reverse characteristics, there are phenomena associated with the forward conducting region that affect the operation of varactor multipliers.^{1,2} The charge-storage effect is particularly important. When the junction becomes forward-biased, minority carriers are injected into both sides of the junction. If these carriers remain in their respective injection regions long enough, they will combine with majority carriers and thus cause a current flow. However, if the minority-carrier lifetime is long with respect to the period of the applied voltage, these carriers will be swept out during the next half-cycle and recombination will not take place. This effect, therefore, represents a recoverable stored charge. An analysis by Leeson¹ of this effect shows that there is an

¹ D. B. Leeson, "Large-Signal Analysis of Parametric Frequency Multipliers," Stanford Electronics Laboratories Technical Report No. 1710-1, Stanford, Cal., 1962.

² G. Luettgenau, J. Williams, and H. Miyahira, "A Practical Approach to the Design of Parametric Frequency Multipliers," Wescon Convention Record, Space Technology Laboratories, Inc., Los Angeles, 1961.

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crease in efficiency when it is used. The amount of the increase is not, however, the major deviation from simple varactor multiplier theory, which does not include the stored-charge effect. The most dramatic effect is the power-handling capability.

It has been shown experimentally that the power input at which maximum efficiency is achieved with an abrupt junction diode ranges from 2 to 6 times that indicated by the simple theory.^{2,3,4} Furthermore, the maximum input power at which an abrupt junction diode can be used at slightly reduced efficiency increases by another factor of 2 or more.⁴ Step-recovery effects also appear to enter into multiplier performance. Step recovery is a result of charge storage that comes about when the minority carriers are returned to the point of origin in a compact bunch; this sudden cessation of current results in a waveform rich in harmonics.⁵ It is possible to enhance certain of these characteristics by shaping the impurity profile. Usually such techniques result in modifying the reverse characteristic also. Varactors are not now characterized in an adequate fashion with respect to the forward region.

Varactor Multiplier Analysis

From the above it is apparent that any general analysis of varactor multipliers must consider the varied nature of the voltage-capacitance characteristic and the effects of forward conduction. Also, the circuit configuration or parameters representing circuit losses must be included. The complexity of the more general problem will not allow its discussion in this treatment; those interested are re-

ferred to Leeson's work.¹ We will limit ourselves to consideration of the charge-controlled circuit, using only the abrupt-junction diode with a square-law characteristic. Conduction in the reverse direction in the diode is sufficiently small to be neglected in this discussion. The effect of forward conduction will not be included, and as a further simplification we will omit the contact potential from Eq. (1) and consider the functional relationship,

$$c = \frac{dq}{dV} = KV^{-1/2}, \quad (2)$$

where V is the magnitude of the reverse voltage. The *incremental* capacitance c , defined above, will be used throughout this discussion.

Common measurement techniques generally employed on varactor diodes lead to values of incremental, rather than total, capacitance. Therefore, the *incremental* capacitance is a more natural definition in discussions involving varactor diodes. The charge-voltage relationship can now be determined from

$$q = \int cdV = \int KV^{-1/2}dV = 2KV^{1/2} + A. \quad (3)$$

Consider the circuit of Fig. 2. The ideal filters in this case allow only ω current in the input port and 2ω current in the output port. Allowing for an arbitrary phase angle ϕ , the current in the varactor is represented by

$$i = I_1 \sin \omega t + I_2 \sin(2\omega t + \phi) = \frac{dq}{dt}. \quad (4)$$

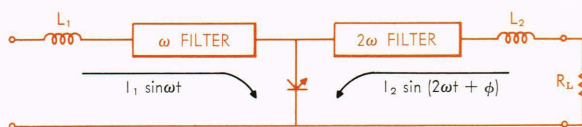


Fig. 2—Charge-controlled varactor doubler.

³ T. M. Hyltin, "Varactor Frequency Multiplier Design," Texas Instruments Technical Seminar, Washington, D. C., May 1964.

⁴ H. C. Lee, "VHF Power Sources Using Varactor Multipliers," RCA Application Note SMA-22, RCA Semiconductor and Materials Division, Somerville, N. J., July 1963.

⁵ G. Schaffner, "High Power Varactor Diodes Theory and Application," *Motorola Monitor*, 2, 1964.

Therefore,

$$q = -\frac{I_1}{\omega} \cos \omega t - \frac{I_2}{2\omega} \cos(2\omega t + \phi) + B, \quad (5)$$

where

$$B = \bar{q} = 2KE_o^{1/2} + A,$$

and E_o represents the voltage across the diode due to the average charge \bar{q} . Equations (3) and (5) lead to

$$V = \left[E_o^{1/2} - \frac{I_1}{2K\omega} \cos \omega t - \frac{I_2}{4K\omega} \cos(2\omega t + \phi) \right]^2. \quad (6)$$

Expanding this expression leads to

$$V = V_0 + V_1 + V_2 + V_3 + V_4, \quad (7)$$

$$V_0 = E_o + \frac{I_1^2}{8K^2\omega^2} + \frac{I_2^2}{32K^2\omega^2}, \quad (7a)$$

$$V_1 = \frac{I_1 I_2}{8K^2\omega^2} \cos(\omega t + \phi) - \frac{I_1 E_o^{1/2}}{K\omega} \cos \omega t, \quad (7b)$$

$$V_2 = \frac{I_2 E_o^{1/2}}{2K\omega} \cos(2\omega t + \phi) + \frac{I_1^2}{8K^2\omega^2} \cos 2\omega t, \quad (7c)$$

$$V_3 = \frac{I_1 I_2}{8K^2\omega^2} \cos(3\omega t + \phi), \quad (7d)$$

and

$$V_4 = \frac{I_2^2}{32K^2\omega^2} \cos(4\omega t + 2\phi). \quad (7e)$$

Consider the expressions for voltage. The time-independent terms include the voltage related to the average charge as well as to the two terms resulting from the currents into the nonlinear device. The sum of these terms represents the bias voltage. If we compare the ω terms, Eq. (7b), to the fundamental current, Eq. (4), we note that the second term is in quadrature with the current and therefore represents a reactance. The first term is in phase with the fundamental current if $\phi = -\pi/2$. For this condition the input power is

$$P_{in} = (V_{rms})(I_{rms}) = \frac{I_1^2 I_2}{16K^2\omega^2}, \quad (8)$$

and $\phi = -\pi/2$ represents maximum P_{in} . The 2ω terms in Eq. (7c) again include a quadrature term and an in-phase term with $\phi = -\pi/2$, $I_2 \sin(2\omega t + \phi) = -I_2 \cos 2\omega t$. Combining Eqs. (4) and (7c), we note that the second harmonic power term is equal to $-P_{in}$; that is, the input power has been transformed to second harmonic power without loss. This is the expected result for our ideal case. It can also be seen that the reactance term at the second harmonic is half that at the fundamental, which is consistent for a doubling of the frequency. It is also interesting to examine the

third and fourth harmonic voltages. The magnitude of the third harmonic component depends upon the product $I_1 I_2$ and is considered a mixing of these two currents in the varactor nonlinearity. The fourth harmonic voltage obviously results from a doubling of the second harmonic component.

We should now consider the possibility of using the above circuit for a tripler by allowing only fundamental and third harmonic currents,

$$i = I_1 \sin \omega t + I_3 \sin(3\omega t + \phi). \quad (9)$$

We note from the above that for this case

$$V \propto [A + B \cos \omega t + C \cos(3\omega t + \phi)]^2. \quad (10)$$

The squared terms ($B^2 \cos^2 \omega t$) and ($C^2 \cos^2 \omega t$) lead to second and sixth harmonic terms (doubling mode). And the cross product leads to second and fourth harmonic terms, the sum and difference (mixing mode). The only fundamental and third harmonic voltage terms result from

$$V_1 = AB \cos \omega t,$$

and

$$V_3 = AC \cos(3\omega t + \phi). \quad (11)$$

These terms are in quadrature with the input and output currents, resulting in no power transformation; therefore, we see that the abrupt junction diode used in the simple charge-controlled circuit cannot be used as a tripler. It can be shown that this diode in a simple charge-controlled circuit can only be used as a doubler. However, as seen in the doubler case, a third harmonic voltage results from the mixing of ω and 2ω terms. If, in addition, we allowed third harmonic current, with an additional arbitrary phase angle, third harmonic power could be generated. This is the argument that leads to the use of "idler" networks to produce higher order multipliers. The 2ω current would not be permitted to flow in the input or output loop, hence an additional loop for this component must be included. Such a loop is called an idler network, and the 2ω current is termed idler current.

Returning to the doubler, I_1 and I_2 are optimized for maximum power by considering the charge on the varactor. The charge as given in Eq. (5) is shown as Fig. 3. The maximum charge is

$$q_{max} = \int_0^{V_B} cdV = 2KV_B^{1/2}, \quad (12)$$

where V_B represents the breakdown voltage. Note that the charge varies from zero to q_{max} and that the average charge is $0.5 \times q_{max}$. By a simple shift of the time axis,

$$q = Q_1 \sin \omega t + Q_2 \sin 2\omega t + KV_B^{1/2}, \quad (13)$$

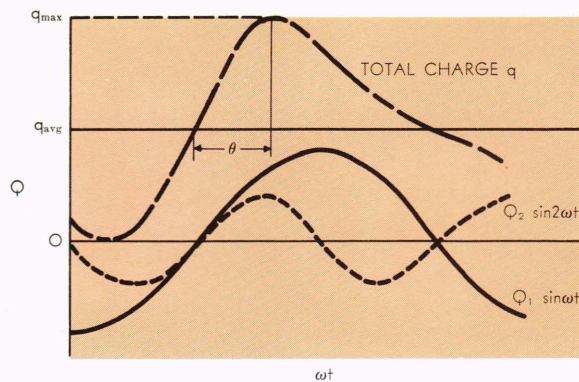


Fig. 3—Varactor charge waveform in a charge-controlled doubler.

where

$$Q_1 = \frac{I_1}{\omega} \text{ and } Q_2 = \frac{I_2}{2\omega}. \quad (14)$$

If we now let θ represent the value of ωt for which $q = q_{max}$, then from Eq. (5), with $q = q_{max}$,

$$KV_{BQ}^{1/2} = Q_1 \sin\theta + Q_2 \sin 2\theta. \quad (15)$$

Also, if we differentiate q with respect to ωt and replace ωt by the angle θ representing the maximum point,

$$Q_1 \cos\theta + 2Q_2 \cos 2\theta = 0. \quad (16)$$

Using these two equations we can express I_1 and I_2 as a function of θ , K , and V_B . Therefore,

$$P \propto I_1^2 I_2 \propto F(\theta).$$

Maximizing the power with respect to θ will enable us to determine I_1 and I_2 , from which we can specify the other parameters. The results are listed below:

$$P_{in} = P_{out} = 2.85 \times 10^{-2} \omega c_{min} V_B^2, \quad (17)$$

$$I_1 = I_2 = 0.77 \omega c_{min} V_B, \quad (18)$$

and

$$R_{in} = R_2 = \frac{9.62 \times 10^{-2}}{\omega c_{min}}, \quad (19)$$

where

$$c_{min} = KV_B^{-1/2} \text{ (capacitance at breakdown)}. \quad (20)$$

The bias voltage and average capacitance are

$$E_b = 0.34 V_B, \quad (21)$$

and

$$c_{avg} = 2c_{min}. \quad (22)$$

Although the foregoing analysis is instructive, it has several limitations. First, we have not dealt

with the varactor series resistance. However, in the case of a simple doubler with high efficiency, suitable results can be obtained by calculating the series resistance loss as

$$\left(\frac{I_1^2}{2} + \frac{I_2^2}{2}\right) R_s. \quad (23)$$

In a similar fashion the circuit loss can also be determined, and the efficiency may then be written as

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}}. \quad (24)$$

For the case of the doubler, including only the loss effect of the varactor series resistance R_s , the efficiency is

$$\eta = 1 - 20.8 \omega c_{min} R_s. \quad (25)$$

The above analysis was first presented by Luettgenau, Williams, and Miyahira.² The results only apply in the case of high-efficiency multiplication because of the manner in which the parasitic resistance is introduced. A more general analysis, which includes the series resistance, was offered by Penfield and Rafuse.⁶ It is interesting to compare the results of the above analysis with the high-efficiency limits resulting from this more general analysis. To make a direct comparison we must introduce another useful varactor parameter. The cutoff frequency is defined as the frequency at which the capacitive reactance is equal to the series resistance. Note that the cutoff frequency is also a function of voltage and that it achieves its maximum value at V_B . If we define ω_c to be the cutoff frequency at the breakdown voltage,

$$\omega_c = \frac{1}{c_{min} R_s}.$$

Using this relationship, the efficiency can be expressed as shown in Table I, which compares the results of the two analyses. The table also includes the results for a single idler tripler and quadrupler.

The analysis of a charge-controlled abrupt junction varactor multiplier using an idler could be approached in the same fashion as the above doubler. In this case one need only introduce the additional current components and proceed through the same steps. It would be of little use to do this here since it would not add particularly to our understanding and because the results of such an analysis are available.² However, several comments on the use of idlers are appropriate.

As has been pointed out, the true square-law device in a charge-controlled circuit can be used

⁶ P. Penfield, Jr. and R. P. Rafuse, *Varactor Applications*, The M.I.T. Press, Cambridge, Mass., 1962.

TABLE I
COMPARISON OF VARACTOR MULTIPLIER PARAMETERS
FOR
DOUBLERS, TRIPLERS, AND QUADRUPLERS

Multiplication Ratio	Parameter	Luetzenau, Williams, and Miyahira*	Penfield and Rafuse†
2	P_{in}	$2.85 \times 10^{-2} \omega c_{min} V_B^2$	$2.86 \times 10^{-2} \omega c_{min} V_B^2$
	R_{in}	$\frac{9.62 \times 10^{-2}}{\omega c_{min}}$	$\frac{9.62 \times 10^{-2}}{\omega c_{min}}$
	R_{out}	$\frac{9.62 \times 10^{-2}}{\omega c_{min}}$	$\frac{9.62 \times 10^{-2}}{\omega c_{min}}$
	c_{avg}	$2 c_{min}$	$2 c_{min}$
	η	$1 - 20.8 \frac{\omega}{\omega_c}$	$1 - 20 \frac{\omega}{\omega_c}$
3	P_{in}	$2.2 \times 10^{-2} \omega c_{min} V_B^2$	$2.38 \times 10^{-2} \omega c_{min} V_B^2$
	R_{in}	$\frac{16.9 \times 10^{-2}}{\omega c_{min}}$	$\frac{13.7 \times 10^{-2}}{\omega c_{min}}$
	R_{out}	$\frac{7.52 \times 10^{-2}}{\omega c_{min}}$	$\frac{6.05 \times 10^{-2}}{\omega c_{min}}$
	c_{avg}	$2 c_{min}$	$2 c_{min}$
	η	$1 - 38 \frac{\omega}{\omega_c}$	$1 - 35 \frac{\omega}{\omega_c}$
4	P_{in}	$1.65 \times 10^{-2} \omega c_{min} V_B^2$	$2 \times 10^{-2} \omega c_{min} V_B^2$
	R_{in}	$\frac{12.7 \times 10^{-2}}{\omega c_{min}}$	$\frac{14.9 \times 10^{-2}}{\omega c_{min}}$
	R_{out}	$\frac{2.3 \times 10^{-2}}{\omega c_{min}}$	$\frac{5.1 \times 10^{-2}}{\omega c_{min}}$
	c_{avg}	$2 c_{min}$	$2 c_{min}$
	η	$1 - 60 \frac{\omega}{\omega_c}$	$1 - 62 \frac{\omega}{\omega_c}$

* Ref. 2
† Ref. 6

only as a doubler. We noted that a single idler at 2ω enables us to realize either a tripler or a quadrupler. To obtain higher multiplication ratios, more than one idler is required. It should also be noted in the case of a quadrupler that a 3ω idler could also be included. It is not possible to state which idler configuration results in the maximum efficiency. The analysis must be undertaken for each case to guide our selection. In the case of higher multiplication ratios the selection of idler frequencies and the number of variations permitted become more complicated. The maximum multiplication ratio obtainable for n idler circuits is 2^{n+1} .

Varactor Multiplier Circuits

SINGLE VARACTOR CIRCUITS—It is relatively easy to obtain a practical circuit that approximates the conditions implied by the analysis. The circuits of Fig. 4 represent a rather straightforward extension of the analysis. In the doubler circuit represented

in Fig. 4A the input is resonated at ω , and matching is accomplished by the adjustment of C_1 . The output circuit is adjusted for 2ω current in the same way. A parallel trap at ω is included in the output loop to reject ω current from the load. This circuit can be built without the ω trap and with efficiencies consistent with the theory. However, fundamental rejection in the output will probably be only on the order of 20 db. For most cases this is not an acceptable level and the trap is required. Note that it is not generally necessary to incorporate a second harmonic trap in the input loop. The amount of 2ω current in this loop is not sufficient to modify the efficiency significantly. An idler loop can be added simply to convert this multiplier to a tripler or quadrupler as shown in Fig. 4B.

The input and output loops of this circuit are identical to those of the doubler if we consider the impedance of L_3 and C_4 to be very high at the output frequency. The idler loop for second harmonic current includes the varactor and the funda-

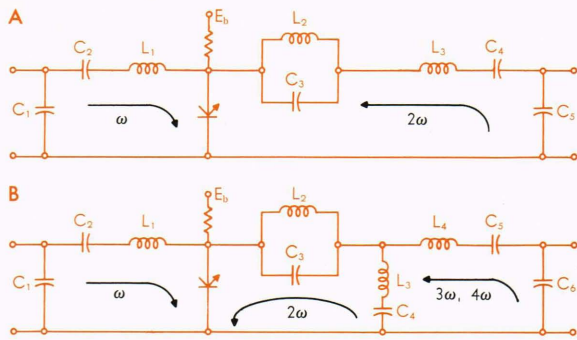


Fig. 4—Single varactor multipliers; (A) doubler, and (B) tripler or quadrupler.

mental trap, L_3 and C_4 . The fundamental trap is included in the idler loop so the impedance of L_3 and C_4 will not directly shunt the varactor at the input frequency. Tests have shown that the efficiency is somewhat lower when the idler loop does not include the fundamental trap. This circuit can be used either as a tripler or a quadrupler. To obtain acceptable rejection of the unwanted harmonics, some extra filtering must be added. Note that L_3 and C_4 are tuned to resonate with the varactor capacitance and the capacitive reactance of the ω trap at 2ω . Rather large second-harmonic voltages exist at the junction of the ω trap and $L_3 - C_4$, because of the large amount of 2ω current through the resulting inductive reactance of L_3 and C_4 . Naturally both 3ω and 4ω voltages are available at the output, the 3ω voltage as a result of the mixing of ω and 2ω currents, and 4ω voltage as a result of doubling the 2ω component.

The simple output circuit shown will not usually give sufficient rejection of the two unwanted components. Parallel traps similar to the ω trap could be added to allow sufficient rejection. Another technique that we have found useful is the use of stubs across the output to obtain appropriate zeros. In the case of a quadrupler, a quarter-wave open stub at ω and a quarter-wave open stub at 2ω are added in parallel with the output. The zeros of this network are at ω , 2ω , 3ω , 5ω , 6ω , etc., with both stubs representing open circuits at the output frequency 4ω . For a tripler, a single half-wave shorted stub at 2ω will offer zeros at 2ω and 4ω , while presenting an open circuit at 3ω . We have found it possible in the VHF region to make such stub arrangements with small-diameter flexible cable, packaged in a small volume, with only small losses. We can see that as higher multiplication ratios are used with this technique, greater amounts of filtering are required. This is one reason for considering circuits using balanced techniques.

BALANCED VARACTOR CIRCUITS—Two balanced doublers are shown in Fig. 5, the simplest of which is Fig. 5A. A push-pull transformer at the input results in fundamental currents of opposite phase in each varactor. The center point of the transformer secondary has a zero at the fundamental and any odd harmonic frequency. Even harmonics are generated at the varactors in phase and are available at the transformer center tap. The second harmonic current from each varactor adds through the output capacitor, which is series-resonant with the self inductance of the transformer and the varactor capacitance. Matching is accomplished by the shunt capacitor at the output.

The second harmonic currents could equally well be generated at the output without making use of the transformer inductance; such a circuit is shown in Fig. 5B. This one, of course, has the disadvantage that it requires a few extra components. The harmonic current relationships are indicated in the figure. We see that the fundamental current circulates around the outer loop, including both varactors and the transformer secondary. If properly balanced, no fundamental current flows in the ground connection, and the center-tap ground connection could be opened without affecting the performance of the circuit.

This circuit has no particular advantage over the other balanced doubler, but is shown as an aid to understanding the circuit of Fig. 6. The latter circuit is a balanced quadrupler, with the harmonic current paths indicated in the figure. The second harmonic current is again returned through the secondary of the transformer as in the doubler circuit of Fig. 5A. In fact this circuit is identical to that in Fig. 5A with respect to ω and 2ω currents. The 4ω current is taken out through the two capacitors and the tuned circuit to the load as indicated. In each of these balanced multipliers it is not necessary to filter against the input frequency at the output because of the symmetry of the cir-

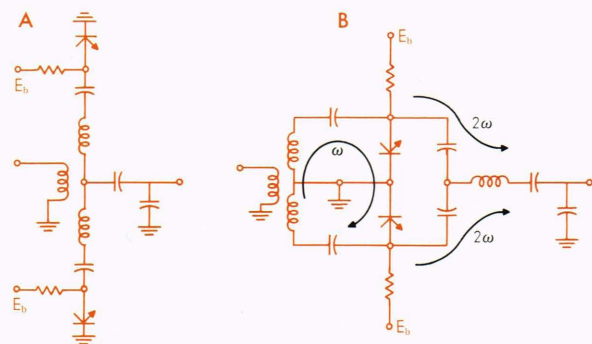


Fig. 5—Balanced varactor doublers.

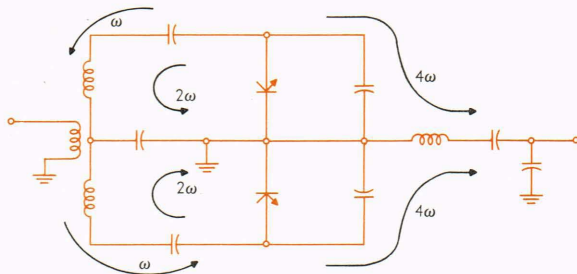


Fig. 6—Balanced varactor quadrupler.

cuit. In the case of the balanced doubler no additional filtering is required. In the case of the quadrupler, ω and 3ω components are balanced out of the output; a 2ω component is still present, however, because of the level of the second harmonic component on the varactor. As in the single-varactor multiplier, this component can be rejected by use of either a parallel trap in series with the output or a series trap in shunt with the output.

One final circuit will complete our discussion of balanced multipliers—the tripler shown in Fig. 7. In this case the varactors are mounted in opposite directions; the fundamental current splits between the two varactors, and even harmonics are generated out of phase while odd harmonics remain in phase. In this case second harmonic current is resonated in the idler loop, as shown resulting in a second harmonic zero at the center point of the idler coil. Third harmonic currents sum at this point and are resonated in the output circuit by the series and shunt capacitors. An inductance is not required in the output loop since the idler loop combination represents an inductance at the output frequency.

Thus far we have not discussed varactor biasing. Generally, varactors are biased in one of two ways: fixed bias or self bias. In most biasing circuits a relatively large resistor is used to reject the R-F currents. When a fixed voltage is applied and slight forward conduction is allowed in the varactor, the bias voltage is actually offset by the voltage drop in the bias resistor. With this arrangement the bias is actually a combination of fixed and self biases. While it is possible to arrange circuits for pure fixed bias, there is no special advantage to this configuration. In the self-bias arrangement a large resistor is connected from the varactor to ground. The bias voltage is obtained by a small rectified current resulting from signal swing into the forward region. One great advantage of the self-biased circuit is that the multiplier is, with this arrangement, completely passive. This is particularly advantageous when both polarity bias voltages would normally be required, as in the tripler of Fig. 7.

Practical Considerations

It is apparent from the above discussion that there are many possible variations in the design of a varactor multiplier. Each application must be considered independently. The primary effort at APL has been in the development of VHF and UHF solid-state transmitters for satellite application. In this area high efficiency, small size, light weight, and high reliability are the prime concerns; the comments following are restricted to this area.

In the design of transmitters requiring ultra-high stability, the basic crystal frequency will generally fall in the low-megacycle region. Multiplication factors of 80 or more are required to raise this frequency into the UHF region. Over the lower range of frequencies both transistor and varactor techniques are suitable. In the upper frequency regions where considerable power is required, transistors are not available. In this area we are clearly restricted to varactor multipliers for any mission requiring the advantages of solid-state techniques.

CIRCUIT SELECTION—Restricting our attention to this area for the moment, and assuming that a multiplication ratio greater than three is required, should one cascade multipliers or attempt a single higher-order multiplier? There is no simple answer to this question; each case must be carefully and individually considered. As an example, assume that a multiplication of 4 is required. At the frequency and power in question, varactors with cut-off frequencies much higher than the operating frequency are available. This is typical at input frequencies in the VHF region and powers of the order of 10 watts. Taking the expressions for efficiency from Table I, the efficiency of two cascaded doublers is

$$\eta = \left(1 - 20\frac{f}{f_c}\right)\left(1 - 20\frac{2f}{f_c}\right),$$

where f is the input frequency of the first doubler and f_c is the varactor cutoff frequency. Neglecting the effect of the $(f/f_c)^2$ term and assuming the same f_c for each diode,

$$\eta = \left(1 - 60\frac{f}{f_c}\right).$$

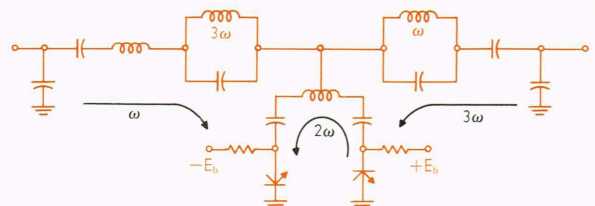


Fig. 7—Balanced varactor tripler.

We observe that this is approximately the same efficiency to be expected from a quadrupler. This is not the whole story, however. It will be remembered that this expression for efficiency does not include the effect of circuit losses. Referring back to the various circuits discussed in the preceding section, it can be seen that a single quadrupler requires less circuitry than a cascade of doublers, a consideration that indicates an efficiency advantage for the quadrupler. This argument applies when the cutoff frequencies available are of the order of 1000 times the operating frequency. Now consider the same problem where the operating frequency is not far removed from the cutoff frequency. The high-frequency efficiency expression for a doubler is⁶

$$\eta = 3.9 \times 10^{-3} \left(\frac{f_c}{f} \right)^2.$$

For a cascade of doublers, square this expression and divide by 2 (the second doubler input frequency is 2f):

$$\eta_{2 \times 2} = 7.6 \times 10^{-6} \left(\frac{f_c}{f} \right)^4.$$

The efficiency for a quadrupler in this case is⁶

$$\eta_{z4} = 5.96 \times 10^{-8} \left(\frac{f_c}{f} \right)^6.$$

Equating these two expressions leads to a ratio of f_c/f of 11. It appears from this consideration that the quadrupler is more efficient than the cascade of doublers for all cases where the cutoff frequency is greater than 11 times the operating frequency. Actually the low-efficiency expressions only apply for f_c/f ratios on the order of 10. And in this region the cascade of doublers appears to be the more efficient. A rather large region exists between these two cases, and it is difficult to determine in any general way which of the two alternatives yields the best efficiency. Efficiency will not be the only factor to consider. The quadrupler with fewer parts will package into less volume and have less weight. Factors relating to tuning sensitivity and performance over a particular range of environmental conditions are generally empirical inputs that will affect the final choice.

Another initial problem is selection of a circuit. What are the relative merits of a balanced circuit compared with a single-ended circuit? One advantage of the balanced circuit has already been considered, namely, the reduction in required filtering. Another advantage that is immediately apparent is the doubled power-handling capability. Another way of considering this advantage is that for a

given power requirement we can select a varactor for a balanced circuit with half the power-handling capability. Since high cutoff frequency and high power capability are opposing functions in the manufacturing process, we can generally select a higher-cutoff-frequency diode for the balanced circuit and thereby obtain a higher efficiency. Balanced circuits also appear to have greater bandwidths than do single varactor circuits. Where cost is a consideration, single varactor multipliers have an obvious advantage.

MULTIPLICATION FACTOR—Returning to our general transmitter problem, the next question that needs to be considered is the frequency at which the transistor power stage will be set. Here again the various alternatives must be considered independently to obtain the best trade-off. If package efficiency is the prime concern, we must determine the decrease in efficiency of the multiplier by increasing the multiplication factor. The question to be answered is, will the cutback in frequency of the power stage allow sufficient increase in its DC efficiency to make the package efficiency higher. The answer is not simple and will generally depend upon empirical data or experienced judgment. Obviously the decision to increase the multiplying factor must result in increased circuitry, size, and weight. When maximum efficiency is the prime consideration, gains can frequently be made by increasing the multiplication ratio, particularly when the power transistor is working near its maximum frequency. When size and weight are the prime considerations, it is generally well to hold to the minimum multiplication ratio. Again, tuning sensitivity, bandwidth, and environmental conditions must be considered.

Considering, now, the other end of our transmitter—the lower-power, lower-frequency multipliers—several alternatives are available. Transistors can be used exclusively, an approach that has several advantages. First, they will generally package in less space than a cascade of high-efficiency varactor multipliers; second, they can be used to obtain gain as we multiply; and third, they are usually less critical to detuning effects since they have larger bandwidths. A second technique would be to attempt the total multiplication in a single-stage varactor and to follow this stage with the required amplifiers. This approach might allow a slight advantage in size, depending on the number of stages required to obtain the necessary signal power. A disadvantage of this technique is that it requires stacking all the gain stages at one frequency, which makes stability problems more difficult. Another approach would be to use high-

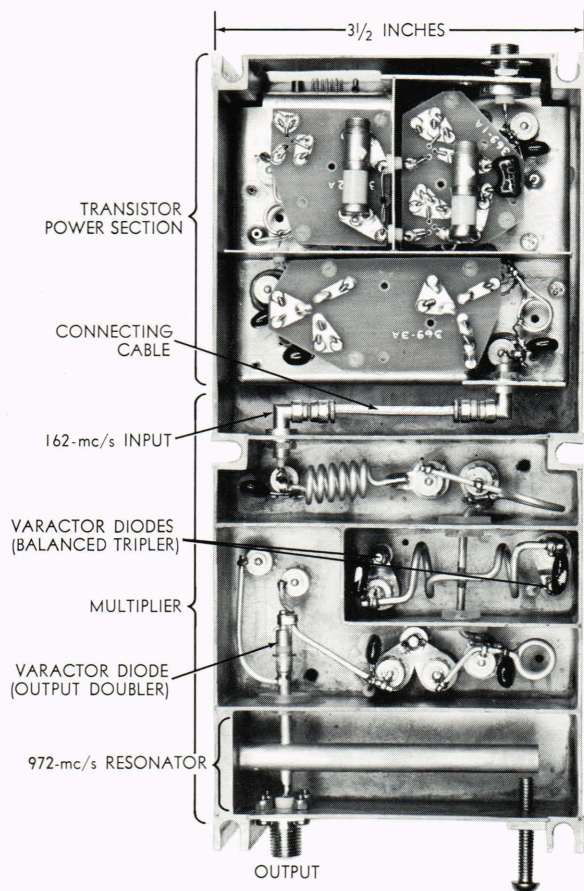


Fig. 8—A transmitter with varactor multipliers designed for the GEOS satellite.

efficiency multipliers and transistor amplifiers together, perhaps interspaced along the multiplier chain. This technique probably would give the best efficiency but require the largest size. We should remember, however, that in the lower power sections of a transmitter the efficiency is not a particularly strong consideration. Generally, we feel that in this area transistor multipliers have a distinct advantage.

MODULATION CHARACTERISTICS — Another factor that cannot be neglected when considering varactor multipliers for use in transmitters is their effect on modulation. Generally, varactor multipliers have nonlinear power-input, power-output characteristics. Therefore, in most cases an AM modulation prior to multiplication cannot be accomplished without increasing the distortion of the modulating signal. Also, the average capacitance of the varactor will change with varying drive level. The resulting detuning effect will lead to a large degree of incidental phase modulation. In some cases where low-level modulation is sufficient and some

reduction in the quality of modulation is acceptable, this technique can be used. For most applications where AM modulation is required, it will be necessary to modulate at the output of the multiplier with some form of loss modulation. Frequency modulation or phase modulation will cause no difficulties if sufficient bandwidth is available so that the sideband distribution will not be altered.

A Satellite Transmitter Application

To illustrate the concepts we have discussed, let us consider a transmitter design recently completed at APL for use in the GEOS satellite. The output section of this transmitter has an input of 5 milliwatts at 54 mc/s and a minimum output of 500 milliwatts at 972 mc/s. The supply voltage is -32 volts, with a maximum DC power input of 5 watts. After considering the various alternatives, it was decided that 162 mc/s represented a good compromise as the frequency for the transistor power section. The completed transistorized section includes an input tripler and three stages of amplification. The power output of the transistor driver is in the range of 1.5 to 1.75 watts. A standard package size used in APL satellites was selected to house the design. The overall package dimensions are $3.5 \times 7.5 \times 1.5$ in.

Internally the package is divided approximately in half, with one side containing the transistor section and the other side the varactor section. For convenience the transistor driver is built into a subchassis which mounts into the main chassis. The varactor multipliers are built directly into the main chassis. Each section can be tested individually; each maintains a 50-ohm input and output impedance; and they are interconnected by a short section of 50-ohm cable. Both sections are completely encapsulated with a low-density foam. The shielding of the transistor section is completed by coating the external surface with a silver-loaded conductive epoxy after a sealer has been applied to the foam. The shielding of the varactor section is completed by the cover plate. Construction details of the package containing the output group can be seen by referring to Fig. 8.

Restricting our attention to the varactor multipliers, a complete schematic is shown in Fig. 9. The balanced tripler used to triple from 162 mc/s to 486 mc/s has already been discussed. The doubler is a variation of those described above. It may be somewhat surprising to some that the output doubler is constructed with lumped circuit elements at this frequency. The reason for this, and also the reason for the circuit modification, is that this particular circuit can be constructed in a very small space. The series resonant circuit on the output side

of the varactor is resonant to the input frequency, thereby effectively grounding that end of the diode at this frequency. The series resonant circuit to ground on the input side of the varactor is approximately resonant at 972 mc/s and performs a similar function. The inductor and capacitor in series with the varactor on the input side tune to resonate with the varactor at the input frequency. It is interesting to note (refer to Fig. 8) that the three inductors referred to above are no more than small pieces of No. 16 silver-plated wire.

Impedance matching is accomplished by the shunt capacitor between the two multipliers. The coaxial resonator at the output is included as a simple filter at 972 mc/s. It can be seen, by referring to Fig. 8, that the output varactor is soldered directly to the resonator tube to establish a good thermal path to conduct heat away from the diode. Also note that both diodes in the tripler have good thermal paths since they are soldered directly to the chassis bottom. These thermal considerations are particularly important in this application.

As an indication of the performance of this multiplier, several curves are included in Fig. 10, showing the variation of power output and efficiency as a function of temperature and drive power. Several of these units have been constructed and tested, with consistently good results.

At this time only one complete package has been subjected completely to the full range of environmental testing. That unit was given full vibration and thermal vacuum testing at design-evaluation levels; all tests have been successfully completed. A final prototype unit is now undergoing tests before being released for the GEOS prototype satellite.

Summary

The unique ability of varactor diodes to make possible highly efficient harmonic generation at

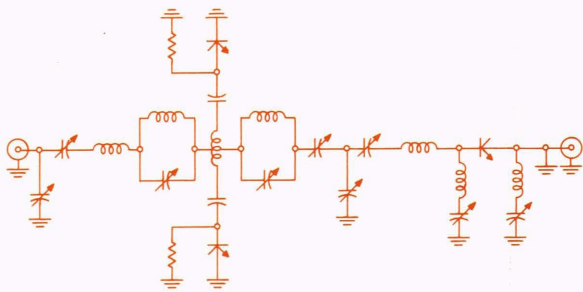


Fig. 9—Schematic of a cascade varactor tripler and doubler for the GEOS-satellite 162-mc/s-to-972-mc/s multiplier.

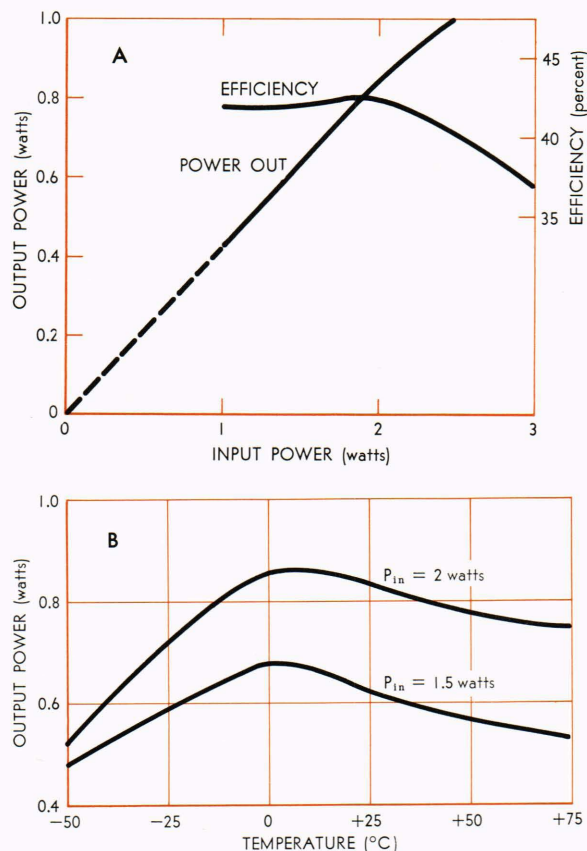


Fig. 10—Performance curves for a 162-mc/s-to-972-mc/s varactor multiplier; (A) power output and efficiency versus power input, and (B) power output versus temperature.

high frequencies will lead to continued expansion in varactor technology. Current trends are toward higher power, higher frequency, and the use of higher multiplication ratios. Continuing investigations will lead to the introduction of new-capacitance nonlinearities suited to particular applications in the field of harmonic generation. Improvement in analytical techniques can be expected to lead to improved characterization of the varactor, such as to define better those characteristics that are not currently included in the model. Some might wonder if advances in high-power, high-frequency transistors will tend to reduce the usefulness of varactor multipliers. Experience to date does not indicate such a trend.

Varactor development will keep pace, and varactors can be expected to maintain a power-frequency capability beyond that of transistors. It must be admitted that as long as frequency multiplication is a useful technique, and wherever efficiency is to be considered, the varactor is assured of a prominent place in the field of solid-state devices.